Video Article

Indium Phosphide Synaptic Device on Silicon to Emulate Synaptic Behavior for Neuromorphic Computing

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Abstract

The protocol presented here describes, in detail, the process flow for a templated liquid-phase growth of crystalline indium phosphide (InP) nanostripes directly on an Si/SiO$_2$ substrate with MoO$_x$ as a thin buffer layer. These InP nanostripes are, then, taken to fabricate InP channel field-effect transistors (FETs) in a scalable manner. Notably, this process allows researchers to obtain InP stripes in the exact geometry and location as may be required for scalable device array fabrication. Further, these FETs are utilized to demonstrate artificial synaptic behavior. The occupation of charge traps in the oxide is modulated by applying gate pulses that mimic pre-synaptic action potentials. The variation of the trapped charge density due to the time-correlated activity of the pre- and postsynaptic neurons results in a threshold voltage shift leading to a change in channel conductance, which is interpreted here as the synaptic weight. A temporal variation of the threshold voltage shift and, thus, of the synaptic weight, arises from the relaxation of traps. Utilizing the time and neuronal activity-dependent synaptic weight change, several important non-linear biological synaptic behaviors are mimicked by the artificial synapse.

Introduction

Currently, a wealth of research and development is taking place for the realization of a time-, energy-, and space-efficient computation for artificial intelligence applications[1]. Multiple hardware implementations of electrical circuits composed of elements and connectivity inspired by relevant components of the human brain are being developed toward realizing this paradigm, which is broadly referred to as neuromorphic computing. A widely accepted abstraction of the human brain for neuromorphic computing consists of neurons as logic units interleaved with synapses as specialized memory links. While neuron and synapse blocks have already been realized by multiple bilevel CMOS logic transistors and capacitors[2,3,4,5,6,7,8,9,10,11,12,13,14,15,16], the next generation circuits will potentially have single-device realizations for each of the neurons and the synapses.

A synapse[17] is a 20- to 40-nm junction between two neurons which aids in the communication of signals between the neurons. The strength of the synapse (better known as its 'weight') determines the amplitude of the current in the postsynaptic neuron generated because of the spiking activity in the presynaptic neuron. These weights are not hard-coded but evolve with time and activity[18]. The non-zero change in the synaptic weight after a neuronal activity is called plasticity and is a measure of the memory retention capacity of the synapse. The synaptic plasticity is, therefore, indicative of the prior neuronal activities and also of the degree to which future neuronal activities would be transduced. Future neuronal activities lead to further synaptic weight change. For the same neuronal activity, the plasticity of the synapse depends on the pre-existing weight of the synapse itself, a phenomenon referred to as metaplasticity[19,20]. Some of the other important weight-updating protocols of the synapse are spike number-dependent plasticity[21] and spike-timing-dependent plasticity (STDP)[22,23,24,25,26]. In spike number-dependent plasticity, the synaptic weight is a function of the number of action potentials arriving at the synapse simultaneously, while STDP demonstrates the synaptic weight change arising from time-correlated activity of the pre- and postsynaptic neurons.

So far, there are few reports on single-device neuron implementation[27,28], whereas single-device synapse implementation has found widespread attention[29,30]. Different material families and device architectures have been studied. Transistors based on controlling the population of charge traps in a floating gate[31] or intrinsically present at the interface or the bulk of the gate dielectric or semiconductor have been demonstrated[21,32,33,34,35]. Several classes of memristive[36] devices based on phase-change[37], and ferroelectric[38,39], ferromagnetic[28], and nanoionic[19,20,40,41,42,43,44,45,46,47,48,49,50,51,52,53,54,55] materials have also been implemented.

In order for neuromorphic computing to be truly ubiquitous while retaining high performance, technologies that would allow a scalable three-dimensional (3-D) integration of high-quality crystalline materials on different substrates are needed. The present 3-D integration approaches are usually based on nanotube networks[56,57,58,59] or nanocrystalline channels[33,37] having low mobility or epitaxial growth, and transfer processes[21,34] having scalability issues. Templated liquid-phase growth is a technique that has been shown to produce large-area, single-crystal compound semiconductor materials on arbitrary, amorphous substrates and in a predesigned location and geometry[60,61,62,63,64,65,66]. In this work, we describe the protocol for the direct growth of a crystalline InP channel on a Si/SiO$_2$ wafer, and the realization of a scalable and potentially Si back-end-compatible array of artificial synapses based on an InP channel FET.

The protocol elaborated herein describes the step-by-step process of fabricating an array of InP nanostripe FETs on an Si/SiO_2 substrate and characterizing them as artificial synapses, a representative result which has been published recently[64].

Protocol

1. Scalable InP Nanostripe FET Fabrication on an Si/SiO_2 Substrate

1. **Preparation of an Si/SiO_2 substrate**
   1. Soak an Si/SiO_2 substrate of 1 x 1 cm^2 sequentially in acetone, isopropyl alcohol, and deionized water for about 30 s each and dry the substrate by blowing N_2 on it.
   2. Clean the substrate by O_2 plasma for a complete removal of organic substances on its surface.
      Note: A 30-s plasma clean with 140 mTorr of O_2 pressure and 30 W of forward power is typically used.
   3. Immediately proceed to step 1.2 or store the substrate in a vacuum desiccator.

2. **InP nanostripe FET pattern lithography**
   1. Spin coat the substrate with lift-off resist (LOR) and perform a pre-exposure bake. For this, spread the LOR at 500 rpm for 5 s and, then, spin coat at 3,000 rpm for 60 s, and pre-exposure bake for 5 min at 175 °C.
   2. Spin coat the substrate with photoresist (PR) and perform a pre-exposure bake. For this (typical process condition), spread the PR at 500 rpm for 5 s and, then, spin coat at 3,000 rpm for 60 s, and pre-exposure bake for 1 min at 110 °C.
   3. Expose the photoresist to ultraviolet light through a contact mask to transfer the nanostripe pattern to the substrate. A typical exposure condition would be a flux of 5 mW/cm^2 for 18 s.
      Note: Rectangular stripes of 2 µm in width were used in this study. This is a limitation by photolithography resolution, and smaller widths can be used if electron beam lithography is performed. Larger widths may also be used to increase the current drive if needed.
   4. Develop the pattern-exposed resist by soaking the substrate in MF-319 developer for 150 s. Rinse it with deionized water and dry it by blowing N_2.

3. **MoO_x/In deposition**
   1. Attach the patterned substrate to the sample stage of the evaporator using polyimide (e.g., Kapton) tape (which has the capability of being cryogenically cooled by heat exchange with liquid nitrogen).
   2. Pump down the chamber to base pressure (typically, 1 to 2 x 10^{-7} Torr). Bring the sample stage to cryogenic temperatures (-150 to -180 °C); for this, either directly flow liquid nitrogen through the stage or flow dry nitrogen cooled in a liquid nitrogen heat exchanger.
   3. Evaporate 5 nm of molybdenum oxide (MoO_3, 99.9995%) at ~0.5 Å/s. Evaporate 100 nm of indium (In, 99.99995%) at ~4 Å/s (in situ with molybdenum oxide or separately).
      Note: If a thermal evaporator is used, such as is done in the present work, alumina-coated molybdenum or tungsten boat may be used in both cases. In the thermal evaporator, a current through the boat is raised to achieve the required evaporation rates observed in the crystal monitor.

4. **Deposit Capping SiO_2**
   1. Attach the MoO_x/In-deposited, patterned substrate to the stage of an e-beam evaporator using polyimide tape.
   2. Pump down the chamber to base pressure (typically, 1 x 10^{-6} Torr). Evaporate 100 nm of SiO_2 (99.99%) at ~4 Å/s.
      Note: If an e-beam evaporator is used, as is done in the present work, the high voltage and gun control are engaged and the rate is observed in the crystal monitor to perform the evaporation.

5. **Transform the In film into InP by a templated liquid phase (TLP) approach**
   1. Immerse the sample in a suitable resist stripper and perform a lift-off of the MoO_x/In/SiO_2 film stack. Rinse the sample using isopropyl alcohol and dry it by blowing N_2. **Figure 1b** is a schematic representation of the sample after this step.
   2. Heat up the sample in vacuum (~7 mTorr) in a single-zone hot-wall tube furnace around 560 °C.
   3. Introduce a mixture gas of 10 sccm of phosphine (99.9995%) and 5 sccm of hydrogen (99.999%) into the growth chamber and set up the chamber pressure around 100 Torr by controlling the exhaust valve.
   4. Maintain the growth temperature and let the InP precipitate out of the liquid In until the entire In template is transformed to InP (typically, 15 min is sufficient). Then, cool down the system to room temperature. **Figure 1c** is a schematic image of the sample after this step.

6. **Source-drain electrodes pattern lithography and metal evaporation**
   1. Repeat steps 1.2.1 through 1.2.4 using a photolithography mask relevant to patterning source-drain electrodes aligned to the InP stripes of the template in step 1.5.4.
   2. Attach the patterned sample from step 1.6.1 to the stage of an e-beam evaporator by polyimide tape. Load Ge, Au, and Ni metal sources in graphite crucibles and pump down the evaporator to a base pressure of ~1 x 10^{-6} Torr.
   3. Engage the high-voltage and gun control of e-beam evaporator, and consecutively evaporate 6 nm of Ge, 10 nm of Au, 80 nm of Ni, and 10 nm of Au.
   4. Immerse the sample in a suitable resist stripper for about 15 min to perform a lift-off to obtain source-drain electrodes. Rinse the sample using isopropyl alcohol and dry it under N_2.
   5. Perform a rapid thermal annealing of the sample in forming gas (5% H_2 and 95% N_2) at an ambient temperature of 380 °C for 15 min.

7. **Gate dielectric oxide layer deposition**
   1. Deposit 60 nm of Al_2O_3 on the entire sample from step 1.6.5 by atomic layer deposition (ALD) at 200 °C, using 97% trimethylaluminum (TMA) and molecular biology grade water (H_2O) as precursors.

8. **Gate electrode lithography and gate metal deposition**

1. Repeat steps 1.2.1 through 1.2.4 using a photolithography mask relevant to patterning the gate electrode on the sample from step 1.7.1.
2. Evaporate by attaching the sample to the stage of an e-beam evaporator using polyimide tape and pumping down to a base pressure of about 1×10^{-6} Torr.
3. Engage the high voltage and gun control of the e-beam evaporator and evaporate 80 nm of Ni at a rate of 4 Å/s.
4. Immerse the sample in a suitable resist stripper and perform a lift-off to obtain gate electrodes. Rinse the sample with isopropyl alcohol and dry it with N_2.

9. **Via lithography and oxide layer wet etching**
    1. Repeat steps 1.2.1 through 1.2.4 using a photolithography mask relevant to patterning source-drain vias on the sample from step 1.8.4.
    2. Etch Al_2O_3 beneath the vias, by hydrofluoric acid solution (HF 50%). A typical process to remove 60 nm of Al_2O_3 is to use 50% $HF:H_2O::1:10$ for 30 s. Rinse the sample using deionized water.
    CAUTION: Hydrofluoric acid is highly corrosive and should be handled with caution while wearing the necessary personal protective equipment.
    3. Strip the resist film in a suitable resist stripper and dry it by blowing N_2 on it. **Figure 1d** is a schematic image of the sample after this step (the end of the fabrication).

2. Synaptic Performance Characterization

1. **Pulse amplitude-dependent plasticity**
    1. Place the sample in the probe station and connect the probes to the gate, source, and drain contact pads.
    2. Connect the gate probe to a voltage pulse generator and the source and drain contacts to source-measurement units (SMUs) of a semiconductor parameter analyzer. Ground the source and apply a constant voltage of 3 V to the drain.
    3. Define the gate voltage as the presynaptic neuron action potential and the source-drain current as the postsynaptic current.
    4. Apply rectangular pulses of varying amplitude and polarity, from -5 V to 5 V, and of a suitable constant pulse width of anything between 500 µs to 5 ms that would mimic a biological pulse time.
    5. Read the source-drain current for each applied pulse for 20 s before and for 40 s after the application of the pulse.
    6. Calculate the synaptic weight change as follows.
        1. Define the short-term plasticity as the difference between the average postsynaptic current (PSC) for 1 s before and after the application of the pulse, normalized to that before the pulse.

        $$\Delta w_{STP} = \frac{<PSC>_{0 \text{ to } 1\text{ s after pulse}} - <PSC>_{0 \text{ to } 1\text{ s before pulse}}}{<PSC>_{0 \text{ to } 1\text{ s before pulse}}}$$

        2. Define the long-term plasticity as the difference between the normalized average PSC between 10 and 40 s after the pulse, and that before the pulse.

        $$\Delta w_{LTP} = \frac{<PSC>_{10 \text{ to } 40\text{ s after pulse}} - <PSC>_{20\text{ s before pulse}}}{<PSC>_{20\text{ s before pulse}}}$$

        3. Define zero plasticity as elasticity, positive plasticity as potentiation, and negative plasticity as depression.
        4. Plot the synaptic weight change *versus* the gate voltage to, ideally, get an exponential dependence: $\Delta w = A \times e^{V_{gp}/V_a}$, where V_{gp} is the peak gate voltage, and V_a is the activation voltage for the traps.

2. **Metaplasticity**
    1. Repeat steps 2.1.1. through 2.1.3.
    2. Define the priming pulse as a presynaptic action potential that changes the initial state of the synapse before the arrival of the main presynaptic action potential.
    3. Design three sets of experiments: without priming pulse, with depressing priming pulse (such as 2.5 V), and with potentiating priming pulse (such as -2.5 V).
    4. For each set, apply the presynaptic action potential priming pulse and start measuring the source-drain current.
    Note: Skip this step for the experiment without priming pulse.
    5. At 10 s, apply varying gate pulses similar to those described in step 2.1.4. Read the source-drain current for 40 s after the application of the main presynaptic pulse.
    6. Repeat step 2.1.6 for each of the three sets of step 2.2.3.

3. **Spike number-dependent plasticity**
    1. Repeat steps 2.1.1 through 2.1.3.
    2. Apply potentiating pulse trains with pulses of fixed amplitude to the presynaptic gate (such as -5 V), of a varying number between 1 and 100, and of a suitable constant pulse width (such as 5 ms pulse width and 5.5 ms period). Repeat step 2.1.5.
    3. Repeat step 2.3.2 but, this time, with depressing pulse trains with pulses of fixed amplitude (such as 5 V).
    4. Plot the long-term and short-term plasticity *versus* the number of action potentials. The trend should initially be increasing and, then, saturating at a higher number of action potentials.

4. **Spike-timing-dependent plasticity**
    1. Repeat step 2.1.1.
    2. Connect the gate and drain probes to separate channels of a voltage pulse generator and the source contact to an SMU of a semiconductor parameter analyzer. Ground the source contact.

3. Define the gate voltage as the presynaptic neuron action potential, the drain voltage as the postsynaptic neuron action potential, and the source-drain current as the postsynaptic current.
   Note: Presynaptic action potential is a bipolar pulse with a small pulse width, such as 10 ms. Reflected postsynaptic action potential is a time-dilated version of the presynaptic action potential with a larger pulse width, such as 100 ms.
4. Choose the presynaptic action potential and the baseline postsynaptic action potential so that they result in elasticity upon the application of presynaptic action potential at the baseline postsynaptic action potential condition.
5. Apply presynaptic action potential. Apply postsynaptic action potential with both time lead and lag.
6. Plot the long-term synaptic weight change *versus* the time difference.
   Note: The trend should be maximum potentiation for minimum positive time correlation and maximum depression for minimum negative time correlation. The synaptic weight change should asymptotically approach elasticity with increasing negative and positive time correlation.

Representative Results

Figure 1a - **1d** schematically show the fabrication of an artificial synaptic device array based on InP nanostripe FETs on an Si/SiO$_2$ substrate as described in the protocol section 1. **Figure 2a** is a schematic of a biological synapse, and the analogous parts in the InP channel FET-based artificial synapse are shown in **Figure 2b**.

The output characteristics of a 2 x 4 array of devices shown in **Figure 3a** - **3h** demonstrate the fair uniformity of device performance across different devices. The average effective mobility extracted from the output and transfer curves of each device is around 200 cm^2/Vs at a 3-V gate voltage overdrive with peak effective mobility around 500 cm^2/Vs, which is more than 10x higher than most carbon nanotube network devices with a peak mobility of 5 - 20 cm^2/Vs.

The hysteretic transfer characteristics shown in **Figure 4a** demonstrate a potentiation for a gate voltage traverse of 0 to -5 to 0 V and a depression for a gate voltage traverse of 0 to 5 to 0 V. On the other hand, as shown in **Figure 4b**, a peak voltage of 0.7 V leads to elasticity with no change in the postsynaptic current (although a peak voltage of -0.7 V still leads to potentiation). A temporal variation of a postsynaptic current showing typical potentiation, depression, and elasticity is shown in **Figure 4c**. Also based on the definition of short-term plasticity and long-term plasticity in the protocol, the synaptic weight change *versus* presynaptic spike amplitude and polarity has been plotted, as shown in **Figure 4d**, and has been fitted with an exponential curve.

To emulate metaplasticity, representative results from a gate voltage pulse train consisting of 10 pulses of ± 4.5 V of 5-ms width and a 6-ms period as the main depressing/potentiating signals are shown in this work. The artificial synapses were either left unprimed or primed with ± 2.5-V depression/potentiation pulse trains. As shown in **Figure 5a**, the -4.5-V pulse train at t = 0 gives a higher chance of a postsynaptic current when succeeding a depressing priming than a potentiating priming. Similarly, the 4.5-V pulse train at t = 0 gives a greater depression when preceded by a potentiating priming than when it is preceded by a depressing priming, as shown in **Figure 5b**. The short-term plasticity for a gate voltage ranging between -5 and 5 V for no priming, depressing priming, and potentiating priming is shown in **Figure 5c**. A consistent trend of increased potentiation for an initially depressed synapse while a decreased potentiation for an initially potentiated synapse is seen. The analogous observation holds for the effect of the synapse to the depressing signal under different initial states.

To emulate the spike number-dependent plasticity, postsynaptic currents have also been plotted for a varying number of spikes, as shown in **Figure 6a**. Both an increased potentiation and a depression with an increasing spike number are observed as expected.

An initially increasing and, thereafter, saturating trend is demonstrated by plotting the long-term and short-term synaptic weight change for an increased number of action potentials, as shown in **Figure 6b** - **6c**. The synaptic weight change initially increases with an increasing number of action potentials, but with a higher number of action potentials, the weight change approaches saturation because of the finite number of trap states accessible by the particular pulse amplitude.

Finally, the emulation of STDP, which is one of the forms of Hebbian learning[60], is demonstrated. The pulse waveforms for pre- and reflected postsynaptic action potentials are shown in **Figure 7a**. The long-term synaptic weight change *versus* t, where t is the relative position between pre- and postsynaptic action potentials, is plotted in **Figure 7b**. It can be observed that the maximum amplitudes of potentiation and depression are achieved at the smallest values of t. For longer time intervals, the amplitude of both potentiation and depression decreases and approaches elasticity as expected.
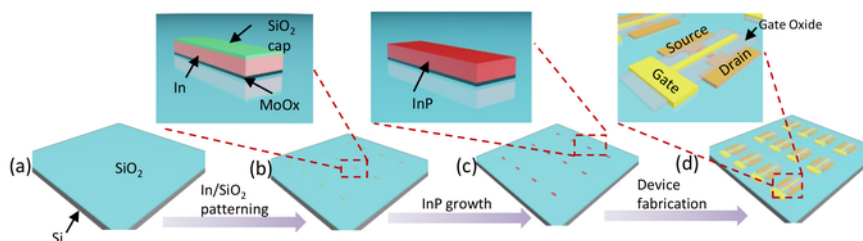
Figure 1: Schematic of TLP growth. (**a** - **d**) Schematic of the TLP growth of single-crystalline InP nanostripe field-effect transistor arrays on Si/SiO$_2$ substrate. Reprinted (adapted) with permission from Kim *et al.*[57], copyright 2018 American Chemical Society. Please click here to view a larger version of this figure.
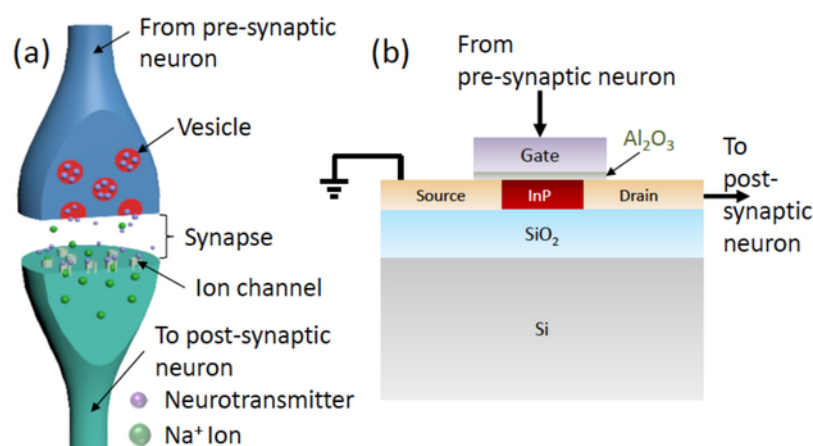
Figure 2: Schematics of a biological synapse and an InP nanostripe FET artificial synapse. (**a**) Schematic of a biological synapse. (**b**) Schematic of an InP nanostripe FET artificial synapse. Reprinted (adapted) with permission from Kim *et al.*[57], copyright 2018 American Chemical Society. Please click here to view a larger version of this figure.
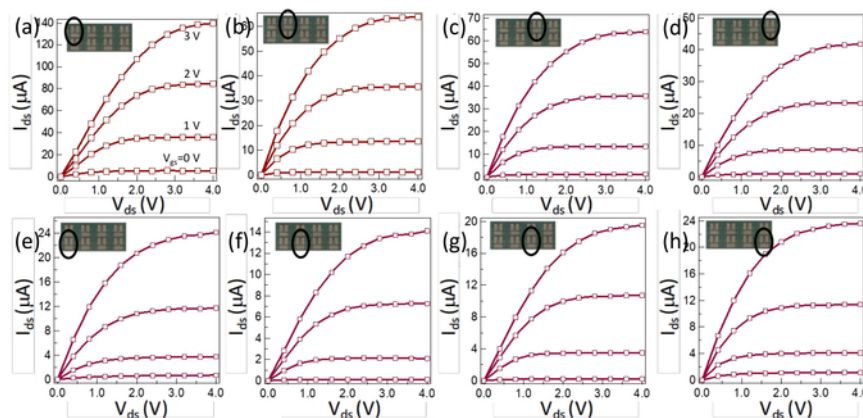

Figure 3: Output characteristics of an array of transistors. (**a** - **d**) These panels show the output characteristics of an array of transistors of 10 μm in length at V_{gs} = 0, 1, 2, 3 V. (**e** - **h**) These panels show the output characteristics of an array of transistor of 25 μm in length at V_{gs} = 0, 1, 2, 3 V. Reprinted (adapted) with permission from Kim *et al.*[57], copyright 2018 American Chemical Society. Please click here to view a larger version of this figure.
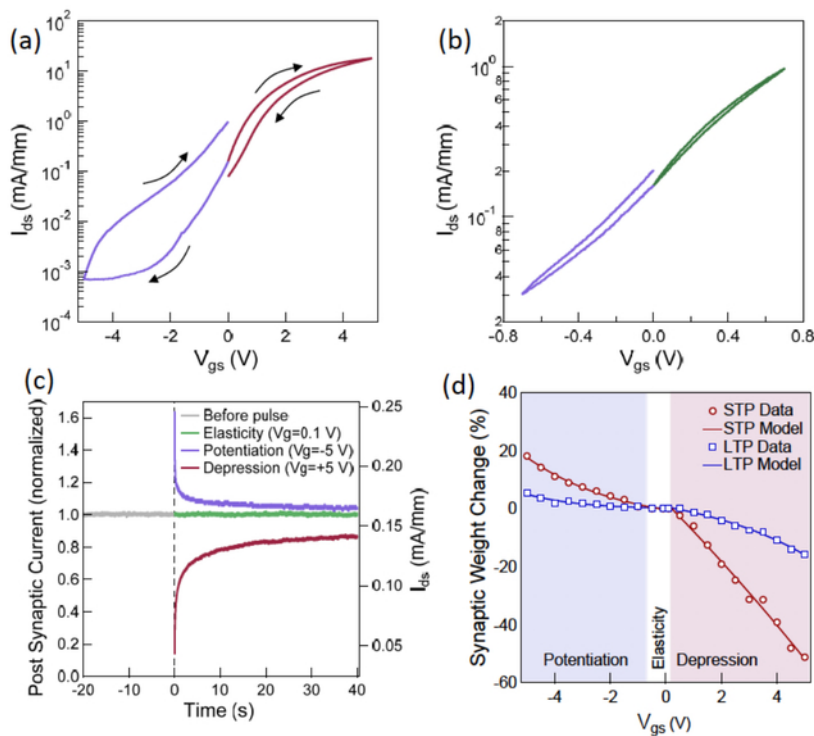
Figure 4: Spike amplitude-dependent plasticity. (**a**) This panel shows hysteretic transfer characteristics showing depression for 5 V and potentiation for -5 V. (**b**) This panel shows hysteretic transfer characteristics showing elasticity for 0.7 V and potentiation for -0.7 V. (**c**) This panel shows the transient postsynaptic current before and after the application of single presynaptic pulse, leading to elasticity (0.1 V), potentiation (-5 V), and depression (+5 V). (**d**) This panel shows short-term and long-term synaptic weight change for different values of a presynaptic voltage pulse. All curves are reported with V_{ds} = 3 V. Reprinted (adapted) with permission from Kim *et al.*[57], copyright 2018 American Chemical Society. Please click here to view a larger version of this figure.
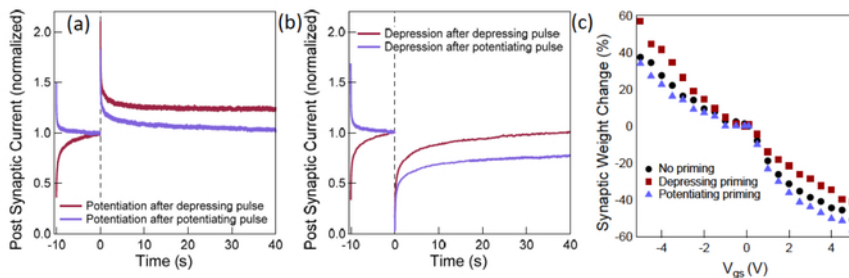
Figure 5: Synaptic metaplasticity. (**a**) This panel shows an increased potentiation of synapse succeeding a depressing priming compared to potentiating priming. (**b**) This panel shows an increased depression of synapse succeeding a potentiating priming compared to depressing priming. (**c**) This panel shows short-term synaptic weight change for different values of presynaptic voltage pulse without priming, and with depressing and potentiating priming. Reprinted (adapted) with permission from Kim *et al.*[57], copyright 2018 American Chemical Society. Please click here to view a larger version of this figure.
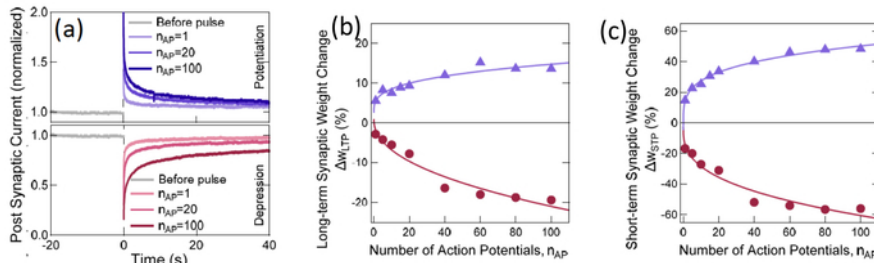
Figure 6: Spike number-dependent plasticity. (**a**) This panel shows a transient postsynaptic current before and after the application of a presynaptic pulse for varying pulse numbers, nAP = 1, 20, 100. (**b**) This panel shows the variation of a short-term synaptic relaxation time constant with a different number of action potentials. The last two panels show (**c**) a long-term and (**d**) a short-term synaptic weight change for a different number of potentiating and depressing action potentials. Reprinted (adapted) with permission from Kim *et al.*[57], copyright 2018 American Chemical Society. Please click here to view a larger version of this figure.
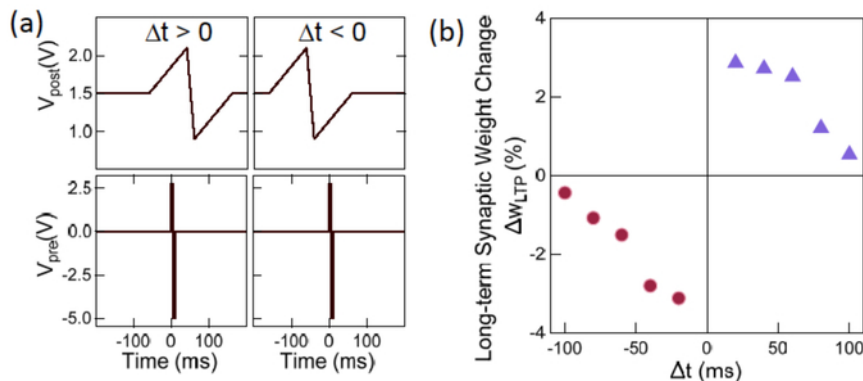
Figure 7: Spike-timing-dependent plasticity. (**a**) This panel shows waveforms representing a back-reflected postsynaptic action potential (upper row) and presynaptic action potential (lower row) for a presynaptic action potential preceding (left column) and succeeding (right column) the reflected postsynaptic action potential. (**b**) This panel shows the long-term synaptic weight change for different values of time, offset between the pre- and postsynaptic action potentials. Reprinted (adapted) with permission from Kim *et al.*[57], copyright 2018 American Chemical Society. Please click here to view a larger version of this figure.

Discussion

Several steps in the protocol deserve discussion. First, in the growth of InP nanostripes, the P flux needs to be tuned as described in previous works[62], to ensure single nucleation in individual channels from which the entire channel grows out, resulting in the single crystallinity of the grown materials. A polycrystalline InP stripe would reduce mobility, thus reducing transconductance, which means the synaptic weight change, which is directly proportional to the transconductance, would also be reduced.

Second, to ensure the wetting of the In templates, the geometry of the template has to be critically maintained. Working within the realms allowed by standard photolithography, a channel width of 2 μm would require 200-nm or thicker In to wet the SiO_2 surface with a SiO_2 capping layer[66]. However, at that thickness, it would be difficult to deplete the entire channel by the gate voltage. Therefore, a thin layer of ~5 nm of MoO_x is deposited, which tunes the surface energies favorably to allow the wetting of 100-nm-thick In.

Third, while an InP-based FET has been demonstrated here as a proof of concept, a multitude of compound semiconductor materials that conform to the TLP growth methodology, such as high-mobility InGaAs, high-bandgap GaN, *etc.*, can potentially be used and chosen according to the application requirements.

Fourth, an important device characteristic is stability over time. Unlike several other material and device classes that have been used to show synaptic behavior, the InP FETs discussed here have been found to be stable over several years despite being stored in normal ambient conditions.

Fifth, an important aspect of the neuromorphic computing paradigm includes hardware implementation with a reduced footprint[1]. It may be noted that this protocol for artificial synaptic devices harnesses the different unique advantages of TLP growth, including scalability and growth in deterministic position and geometry, to obtain single-device synaptic implementation. Although the devices shown here are in the micron scale for proof-of-concept demonstration, it can be easily realized that, with existing fabrication capabilities, the footprint is significantly reduced to the nanometer scale in the future.

Sixth, arguably the most important aspect of neuromorphic computing is energy efficiency in handling large datasets. This can be achieved by an optimal choice of the pulse width and amplitude. It may be noted that, here, hundreds of microseconds to a few millisecond scale pulse widths

are chosen, which conforms to biological neuronal spiking standards. The pulse amplitudes are relatively higher than usual, stemming from the relatively thick gate oxide used here. However, this can also be taken care of, by suitably designing a scaled device.

Disclosures

The authors have nothing to disclose.

Acknowledgements

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