Video Article

Developing High Performance GaP/Si Heterojunction Solar Cells

Chaomin Zhang[1], Ehsan Vadiee[1], Som Dahal[1], Richard R. King[1], Christiana B. Honsberg[1]

[1]School of Electrical, Computer, and Energy Engineering, Arizona State University

Correspondence to: Chaomin Zhang at chaomin.zhang@asu.edu

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Abstract

To improve the efficiency of Si-based solar cells beyond their Shockley-Queisser limit, the optimal path is to integrate them with III-V-based solar cells. In this work, we present high performance GaP/Si heterojunction solar cells with a high Si minority-carrier lifetime and high crystal quality of epitaxial GaP layers. It is shown that by applying phosphorus (P)-diffusion layers into the Si substrate and a SiN_x layer, the Si minority-carrier lifetime can be well-maintained during the GaP growth in the molecular beam epitaxy (MBE). By controlling the growth conditions, the high crystal quality of GaP was grown on the P-rich Si surface. The film quality is characterized by atomic force microscopy and high-resolution x-ray diffraction. In addition, MoO_x was implemented as a hole-selective contact that led to a significant increase in the short-circuit current density. The achieved high device performance of the GaP/Si heterojunction solar cells establishes a path for further enhancement of the performance of Si-based photovoltaic devices.

Video Link

The video component of this article can be found at https://www.jove.com/video/58292/

Introduction

There has been a continuing effort on the integration of different materials with lattice mismatches in order to enhance overall solar cell efficiency[1,2]. The III-V/Si integration has the potential to further increase the current Si solar cell efficiency and replace the expensive III-V substrates (such as GaAs and Ge) with a Si substrate for multijunction solar cell applications. Among all III-V binary material systems, gallium phosphide (GaP) is a good candidate for this purpose, as it has the smallest lattice-mismatch (~0.4%) with Si and a high indirect bandgap. These features can enable high-quality integration of GaP with Si substrate. It has been theoretically shown that GaP/Si heterojunction solar cells could enhance the efficiency of conventional passivated emitter rear Si solar cells[3,4] by benefiting from the unique band-offset between GaP and Si (ΔE_v ~1.05 eV and ΔE_c ~0.09 eV). This makes GaP a promising electron selective contact for silicon solar cells. However, in order to achieve high-performance GaP/Si heterojunction solar cells, a high Si bulk lifetime and high GaP/Si interface quality are required.

During the growth of III-V materials on a Si substrate by molecular beam epitaxy (MBE) and metalorganic vapor phase epitaxy (MOVPE), significant Si lifetime degradation has been widely observed[5,6,7,8,9]. It was revealed that the lifetime degradation mainly happens during the thermal treatment of the Si wafers in the reactors, which is required for surface oxide desorption and/or surface reconstruction before the epitaxial growth[10]. This degradation was ascribed to the extrinsic diffusion of contaminants originated from the growth reactors[5,7]. Several approaches have been proposed to suppress this Si lifetime degradation. In our previous work, we have demonstrated two methods in which the Si lifetime degradation can be significantly suppressed. The first method was demonstrated by the introduction of SiN_x as a diffusion barrier[7] and the second one by introducing the P-diffusion layer as a gettering agent[11] to the Si substrate.

In this work, we have demonstrated high-performance GaP/Si solar cells based on the aforementioned approaches to mitigate the silicon bulk lifetime degradation. The techniques used to preserve the Si lifetime can have broad applications in multijunction solar cells with active Si bottom cells and electronic devices such as high-mobility CMOS. In this detailed protocol, the fabrication details of GaP/Si heterojunction solar cells, including Si wafer cleaning, P-diffusion in the furnace, GaP growth, and GaP/Si solar cells processing, are presented.

Protocol

CAUTION: Please consult all relevant material safety data sheets (MSDS) before dealing with chemicals. Please use all appropriate safety practices when performing a solar cell fabrication including the fume hood and personal protective equipment (safety glasses, gloves, lab coat, full-length pants, closed-toe shoes).

1. Si Wafer Cleaning

1. Clean Si wafers in Piranha solution (H_2O_2/H_2SO_4) at 110 °C.

1. To produce Piranha solution, fill the acid bath (high-density polyethylene tank and hereafter) with 15.14 L of H_2SO_4 (96%) and then 1.8 L of H_2O_2 (30%).
2. Wait for the temperature of the solution to stabilize at 110 °C.
3. Place 4-inch-diameter, float-zone (FZ), n-type, and double-side-polished Si wafers in a clean 4" wafer cassette (polypropylene and hereafter), and place the boat in the Piranha bath for 10 min.
4. Rinse for 10 min with deionized (DI) water.

2. Clean Si wafers with RCA cleaning solution at 74 °C.
   1. Prepare a diluted solution of HCl:H_2O_2. Fill the acid bath with 13.2 L of DI H_2O and 2.2 L of HCl. Spike the solution with 2.2 L of H_2O_2 and turn on the heater.
   2. Wait for the temperature of the solution to stabilize at 74 °C before use.
   3. Put Si wafers in a clean 4" wafer cassette and place wafers in the RCA solution for 10 min.
   4. Rinse with DI water for 10 min.

3. Clean Si wafers in Buffered Oxide Etch (BOE) solution.
   1. Pour 15.14 L of BOE solution in the acid bath.
   2. Place the 4" wafer cassette in the bath for 3 min.
   3. Rinse for 10 min with DI water.
   4. Dry the wafer by dry N_2.

2. P-diffusion in the Diffusion Furnace

1. Put a cleaned wafer in a diffusion quartz boat.
2. Load it into a quartz tube that has a base temperature of 800 °C. Ramp the furnace temperature to 820 °C in the N_2 environment. At 820 °C, start flowing the N_2 carrier gas that bubbles through phosphorous oxychloride ($POCl_3$) at 1000 sccm. After 15 min, turn off the N_2 carrier gas and ramp the temperature down to 800 °C before taking the samples out.
3. Place the samples in a BOE solution for 10 min to remove phosphorus silicate glass (PSG) and then perform a 10-min rinse in DI water.

3. SiN_x coating by PECVD

1. Put the wafer in a clean boat and dip it in a BOE bath for 1 min to remove the native oxide on the surface.
2. Rinse for 10 min with DI water.
3. Dry the wafer with a dry N_2 gun.
4. Place the Si wafer on a clean Si carrier (156 mm monocrystalline Si).
5. Load the sample into the plasma enhanced chemical vapor deposition (PECVD) chamber.
6. Deposit 150 nm-thick (38.5 s) SiN_x at 350 °C in the chamber. Deposit SiN_x at 300 W RF power with a base pressure of 3.5 Torr and 60 sccm of SiH_4 as a silicon source and 60 sccm of NH_3 as a N source (2000 sccm of N_2 was used as a diluent).
   1. Confirm the growth rate of SiN_x (3.9 nm/s) by depositing SiN_x films with different deposition times on polished wafers and measure the thicknesses by variable angle spectroscopic ellipsometry (VASE).

4. GaP Growth by MBE

1. After SiN_x deposition, load the wafer into the MBE chamber.
2. Outgas in the introductory chamber (180 °C for 3 h), then outgas in the buffer chamber (240 °C for 2 h). Load in to the growth chamber and bake at 850 °C for 10 min.
3. Decrease temperature to 580 °C. Increase Ga effusion cell temperature to produce ~2.71×10^{-7} Torr beam-equivalent pressure (BEP) and Si effusion cell temperature to 1250 °C.
4. Adjust the p-valved cracker positioner to achieve ~1.16×10^{-6} Torr BEP. Open the Ga, P, and Si shutters and grow 25 nm-thick GaP with an interrupted growth method (10 cycles of 5 s open and 5 s closed) followed by 121 s of unshuttered growth (*i.e.,* open Ga and p shutters simultaneously).
5. Decrease the substrate temperature to 200 °C and unload the sample from the vacuum chamber.

5. Remove Back n+ and SiN_x Layers by Wet Etching

1. Cover the GaP surface with a protective tape to protect it from the HF damage.
2. Prepare ~300 mL of 49% HF solution in a plastic beaker.
3. Place the sample in the HF solution for 5 min to fully remove the SiN_x layer.
4. Remove the protective tape, rinse with DI water, and dry by N_2.
5. Cover the GaP surface with a new protective tape.
6. Prepare HNA solution in a plastic beaker (a mixture of hydrofluoric acid (HF) (50 mL), nitric acid (HNO_3) (365 mL), and acetic acids (CH_3COOH) (85 mL)) at room temperature.
   CAUTION: Carefully place the wafer in the solution to avoid HNA penetrating into the GaP surface.
7. Put the sample in the HNA solution for 3 min.
8. Remove the protective tape and rinse by DI water. Dry by N_2.

6. Hole-Selective Contact Formation on the Bare Si Side

1. Cleave the wafer with a diamond pen into four quarters.
2. Thoroughly clean the samples in a DI water tank.
3. Clean the samples in a BOE bath for 30 s to remove the native oxide from the surface.
4. Rinse in the wafers in DI water and then dry by N_2.
5. Deposit a 50 nm-thick a-Si: H by PECVD on one of the samples to check the Si lifetime.
    1. Deposit the a-Si: H layer at 60 W RF power with a pressure of 3.2 Torr and 40 sccm of SiH_4 as the silicon source (200 sccm of H_2 was used as a diluent).
    2. Confirm the growth rate of a-Si: H (1.6 nm/s) by depositing a-Si films with different deposition times on polished wafers and measuring the thickness with VASE.

6. Deposit (i)a-Si (9 nm) and (p+)a-Si (16 nm) on the etched (front) side of a separate Si sample by PECVD.
    1. Deposit the p-type a-Si layer at 37 W RF power with a pressure of 3.2 Torr and 40 sccm of SiH_4 as the silicon source and 18 sccm of $B[CH_3]_3$ as the boron dopant (197 sccm of H_2 was used as a diluent).
    2. Confirm the growth rate of p-type a-Si (2.0 nm/s) by depositing a-Si films with different growth times on the polished wafers and measuring the thicknesses with VASE.

7. Deposit a 9 nm-thick MoO_x layer at the room temperature by the thermal evaporation from a MoO_3 (99.99%) source with a deposition rate of 0.5 Å/s.

7. External Contact Formation

1. Deposit 75 nm-thick Indium Tin Oxide (ITO) (In_2O_3/SnO_2 = 95/5 (weight percent), 99.99%) layers on the GaP side of the samples by RF sputtering (RF power of 1 kW and pressure of 5 Torr) with an oxygen flow rate of 2.2 sccm.
2. Unload the samples and turn them over. Then use the mesa shadow mask on the samples for ITO mesa deposition.
3. Deposit 75 nm-thick ITO by RF sputtering. Deposit 200 nm-thick silver (RF power of 1 kW and pressure of 8 Torr) for the fingers covering the finger shadow mask. Deposit 200 nm-thick silver on the GaP side of the samples as the back contact.
4. Anneal the samples in a furnace under atmospheric pressure at 220 °C.

Representative Results

Atomic force microscopy (AFM) images and high-resolution x-ray diffraction (XRD) scans, including the rocking curve in the vicinity of the (004) reflection and the reciprocal space map (RSM) in the vicinity of (224) reflection, were collected for the GaP/Si structure (**Figure 1**). The AFM was used to characterize the surface morphology of the MBE-grown GaP and XRD was used to examine the crystal quality of GaP layer. The effective minority-carrier lifetime of the GaP/Si structure and Si bulk were measured to examine the effectiveness of the lifetime preserving methods used in this work. External quantum efficiency (EQE), surface reflection, pseudo light J-V (Suns-Voc), and light J-V of the GaP/Si final devices were collected (**Figure 2**). The internal quantum efficiency (IQE) was generated from the reflection corrected EQE data. The light and pseudo J-V parameters are listed in **Table 1**. Efficiencies of 13.1% and 14.1% with an open-circuit voltage (V_{oc}) of 618 mV and 598 mV are achieved from Structure A and B, respectively. The MoO_x layer in Structure B as a hole-selective contact performed better than better than the a-Si: H in Structure A.

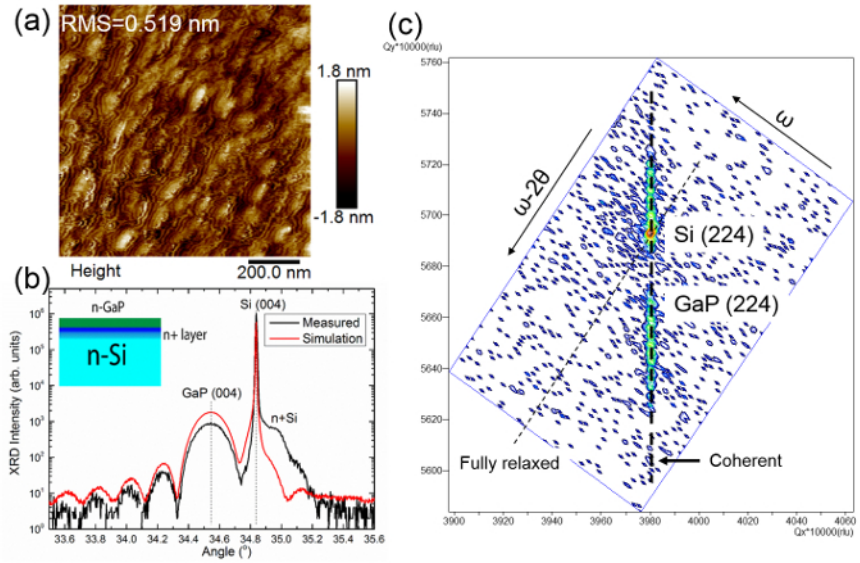

Figure 1: Characterization of the GaP layer of the GaP/Si structure. (a) 1 x 1 μm^2 AFM image of the 25 nm-thick GaP surface. (b) The coherent double crystal (DC) ω-2θ rocking curve (black) in the vicinity of Si and GaP (004) reflections (a fitted curve (red) of the structure is also presented). (c) Reciprocal space map of (224) diffraction spots. Please click here to view a larger version of this figure.

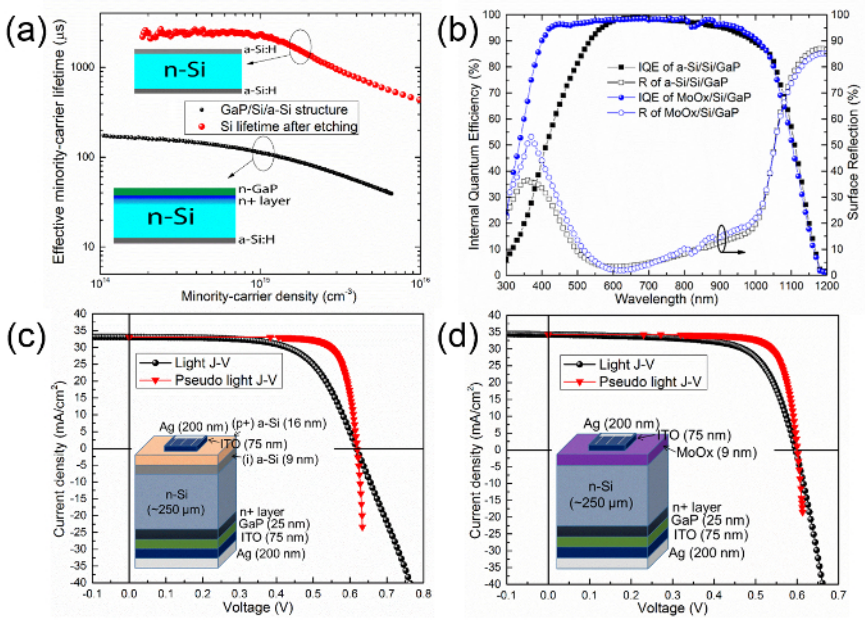

Figure 2: Electrical characteristics of the GaP/Si heterojunction devices. (a) The effective minority-carrier lifetime of GaP/Si structure (black dots) and Si bulk lifetime (red dots). (b) The IQE and surface reflection spectra of a-Si/Si/GaP (Structure A) (black) and MoO_x/Si/GaP (Structure B) (blue). (c) Light J-V (black) and pseudo light J-V (red) of a-Si/Si/GaP device. (d) Light J-V (black) and pseudo light J-V (red) of MoO_x/Si/GaP device. Please click here to view a larger version of this figure.

	V_{OC}	J_{SC}	FF	FF_0	W_{OC}	η	$η_0$
	(mV)	(mA/cm^2)	(%)	(%)	(mV)	(%)	(%)
Structure A	618	33.1	64	80	522	13.1	16.5
Structure B	598	34.3	69	80	542	14.1	16.9

Table 1. Light and pseudo J-V values for GaP/Si heterojunctions solar cells.

Discussion

A nominal 25 nm-thick GaP layer was epitaxially grown on a P-rich Si surface via MBE. To grow a better quality of GaP layer on Si substrates, a relatively low V/III (P/Ga) ratio is preferable. A good crystal quality of GaP layer is necessary to achieve high conductivity and low density of recombination centers. The AFM root-mean-square (RMS) of the GaP surface is ~0.52 nm showing a smooth surface with no pits, indicative of high crystal quality with a low threading dislocation density (**Figure 1a**). Further, pendellosung fringes were observed from the ω-2θ rocking curve (**Figure 1b**) indicative of smooth interfaces. The full width at half maximum (FWHM) of the GaP peak measured from the triple crystal ω rocking curve is ~14 arcsec and the threading dislocation density calculated is ~2×10^6 cm^{-2}. The RSM (**Figure 1c**) in the vicinity of (224) diffraction spots of the GaP/Si sample shows coherent GaP and Si peaks, which indicates GaP is fully strained to the Si substrate with good crystalline quality.

The critical step of achieving high-performance Si-based solar cells is to maintain high Si minority-carrier lifetimes throughout the deposition of GaP. It is shown that by inserting the n+ layer before the GaP growth, the Si bulk lifetime can be well-maintained (up to a milliseconds level). In addition, the GaP/Si lifetime was measured to be ~100 µs after GaP growth in the MBE chamber. The achieved high lifetime of Si indicates a promising device performance (as shown in the **Figure 2c**). The light and pseudo J-V parameters for GaP/Si heterojunctions solar cells (a-Si/Si/GaP (Structure A) and MoO_x/Si/GaP (Structure B)) are listed in **Table 1**, measured under an AM1.5G condition with irradiation intensity of 1 kW m^{-2}. While ITO and Ag were applied as the contact layers to the GaP layer in this work, however, to achieve better performance of GaP/Si solar cells, it is recommended to optimize ITO thickness, transparency, and its conductivity.

In this work, MoO_x was also used as a hole selective contact to further improve the carrier collection efficiency at short wavelengths. Benefitting from the higher bandgap of MoO_x compared to the a-Si layers, the IQE shows a boost at the short wavelength regime (300 - 600 nm). The MoO_x/Si/GaP solar cell demonstrated a better performance than the best performing MoO_x/Si solar cells reported in the literature[12] without inserting the passivation layer between MoO_x and Si interface.

Although a high Si bulk lifetime can be achieved from the aforementioned approach, the minority-carrier lifetime of GaP/Si structure is still not comparable to a-Si passivated structures, which implies that the GaP layer quality should be further improved. The demonstrated approach which requires a diffusion step and SiN_x coating layer could affect the surface quality of the Si; hence, the subsequent GaP crystal quality can be impacted. Furthermore, x-ray photoelectron spectroscopy (XPS) and secondary-ion mass spectrometry (SIMS) can be conducted to investigate the P-diffusion profile in this structure.

In this work, we have demonstrated the high-performance GaP/Si heterojunction solar cells by inserting n+ layers into Si substrates before the GaP growth. This protocol can be applied to maintain a high minority-carrier lifetime of Si while epitaxially growing not only GaP (presented here) but also to other III-V or II-VI materials to achieve heterojunction devices. Furthermore, multijunction solar cells with high-performance Si bottom cells can be realized by this approach.

Disclosures

The authors have nothing to disclose.

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