Video Article

A Standard and Reliable Method to Fabricate Two-Dimensional Nanoelectronics

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Abstract

Two-dimensional (2D) materials have attracted huge attention due to their unique properties and potential applications. Since wafer scale synthesis of 2D materials is still in nascent stages, scientists cannot fully rely on traditional semiconductor techniques for related research. Delicate processes from locating the materials to electrode definition need to be well controlled. In this article, a universal fabrication protocol required in manufacturing nanoscale electronics, such as 2D quasi-heterojunction bipolar transistors (Q-HBT), and 2D back-gated transistors are demonstrated. This protocol includes the determination of material position, electron beam lithography (EBL), metal electrode definition, *et al*. A step by step narrative of the fabrication procedures for these devices are also presented. Furthermore, results show that each of the fabricated devices has achieved high performance with high repeatability. This work reveals a comprehensive description of process flow for preparing 2D nano-electronics, enables the research groups to access this information, and pave the way toward future electronics.

Video Link

The video component of this article can be found at https://www.jove.com/video/57885/

Introduction

Since past decades, mankind has been experiencing rapid downscale in the size of transistors and, consequently, an exponential increase in the number of transistors in integrated circuits (ICs). This maintains the continuous progress of silicon-based complementary metal-oxide semiconductor (CMOS) technology[1]. Moreover, this current trend in the size and performance of fabricated devices are still on-track with Moore's law, which states that the number of transistors on electronic chips, as well as their performance, doubles roughly every two years[2]. CMOS transistors are present in most, if not all, of the electronic devices available in the market and thus making it an integral part of human lives. Due to this, there are continuous demands for improvements in chip size and performance which have been pushing the manufacturers to keep following the Moore's law track.

Unfortunately, Moore's law appears to be nearing its end due to the amount of heat generated as more silicon circuitry is squeezed into a small area[2]. This calls for new types of materials that can provide the same, if not better, performance as silicon and, at the same time, can be implemented in a relatively smaller scale. Recently, new promising materials have been subjects of many material science researches. Such materials as one-dimensional (1D) carbon nanotubes[3,4,5,6,7], 2D graphene[8,9,10,11,12], and transition metal dichalcogenides (TMDs)[13,14,15,16,17,18], are good candidates that can be used as substitute for the silicon-based CMOS and continue the Moore's law track.

Fabrication of small-scale devices requires careful determination of the material's location to successfully proceed to the other fabrication techniques such as lithography and metal electrode definition. So, the method presented in this paper was designed to address this need. Compared to the traditional semiconductor fabrication techniques[19], the approach presented in this paper is tailor-fitted to the development of small-scale devices which needs more attention in terms of finding the location of the material. The aim of this method is to reliably fabricate 2D nanomaterial devices, such as 2D back-gated transistors and Q-HBTs, using standard fabrication processes. This can serve as a platform for future nanodevice developments as it paves the way towards the production of future advanced nano-scale devices.

In the proceeding section, the fabrication processes for 2D materials-based devices namely, the Q-HBT and 2D back-gated transistor are discussed in detail. Electron beam patterning combined with material location determination and metal electrode definition comprises the protocol since they are required in both mentioned processes. Part 1 discusses the step-by-step fabrication process of Q-HBTs[20]; and part 2 demonstrates a universal approach to obtain chemical vapor deposition (CVD) molybdenum disulfide (MoS_2) back-gated transistors from transfer to lift-off[21], which has been completely shown in the article. The detailed process flow is illustrated in (**Figure 1**).

Protocol

1. 2D Quasi-heterojunction Transistors Fabrication Process

1. Prepare commercial c-plane sapphire.
    1. Wash the whole single-side polished sapphire (2-inch) with acetone.
    2. Rinse the sapphire substrate with isopropyl alcohol.

2. Grow MoS_2 on sapphire substrate using CVD in a hot-wall furnace.
    1. Place 0.6 g of molybdenum trioxide (MoO_3) powder in a quartz boat located at the heating zone center of the furnace. Put the sapphire substrate downstream next to the quartz boat containing the MoO_3 powder.
    2. Prepare sulfur (S) powder in a separate quartz boat at the upstream side of the furnace. Maintain its temperature at 190 °C during the reaction.
    3. Use argon (Ar = 70 sccm, 40 Torr) gas flow to bring the S and MoO_3 vapors to the sapphire substrate while heating the center zone to 750 °C.
    4. Keep the heating zone, after reaching the desired growth temperature of 750 °C, for 15 min and then naturally cool down the furnace to room temperature.

3. Perform EBL.
    NOTE: A thin Au of about 5 nm was deposited by the sputtering for discharging during all EBL processes on sapphire substrate
    1. Identify, using an optical microscope, an area where MoS_2 monolayer flakes are observed, then design the stripe pattern layout for that specific area using a design software (AutoCAD).
    2. Spin-coat photoresist (PR), for example polymethyl methacrylate (PMMA) or P015, on top of the sample at 2000 rpm for 60 s (room temperature). Ensure that the PR has covered the entire sample after spin coating.
    3. Heat the sample (Soft Bake) at 100 °C for 90 s in order to evaporate the solvents in the PR and enhance the adhesion.
    4. Convert the pattern layout in step 1.3.1 into a specific file (example: GDS file), and upload it in the EBL software.
    5. Determine the ideal dose of electron beam based on the width of the lines in the layout.
        NOTE: For line width narrower than 1 µm, the ideal dose of electron beam is 110 µC/cm^2; for 1 to 5 µm line width, the dose is 100 µC/cm^2; and for line width wider than 5 µm, the dose is 80 µC/cm^2.
    6. Start exposing the sample to electron beam.
    7. Apply post-exposure bake (PEB) on the sample after the exposure in order to reduce the standing wave effects. Heat the sample at 120 °C for 90 s.
    8. Use tetramethylammonium hydroxide (TMAH) 2.38% as developer. Immerse the sample to TMAH for 80 s. Wash out the TMAH with 200 mL of deionized water for 10 s.
    9. Examine if the pattern is well developed by optical microscopy.
    10. Conduct hard bake to get rid of extra water in PR. Heat the sample at 110 °C for 90 s.

4. Define the stripe structures using 50 W oxygen (O_2) plasma etching (1^{st} etching) for 30 s to 2 min and remove PR using 50 mL of acetone.
5. Grow tungsten diselenide (WSe_2) using CVD on the target location, which will result in a preferred growth of WSe_2 layer between the already existing MoS_2 stripes on the sapphire substrate.
    1. Place 0.6 g of tungsten trioxide (WO_3) powder in a quartz boat located at the heating zone center of the furnace. Put the sapphire substrate downstream next to the quartz boat containing the WO_3 powder.
    2. Prepare selenium (Se) powder in a separate quartz boat at the upstream side of the furnace. Maintain its temperature at 260 °C during the reaction.
    3. Use Ar/H_2 (Ar = 90 sccm, H_2 = 6 sccm, 20 Torr) gas flow to bring the Se and WO_3 vapors to the sapphire substrate while heating the center zone to 925 °C.
    4. Keep the heating zone, after reaching the desired growth temperature of 925 °C, for 15 min and then naturally cool down the furnace to room temperature.

6. Fabricate the metal pad arrays and alignment marks.
    1. Overlay the patterns of metal pad arrays and alignment the marks using photolithography patterning technique.
    2. Deposit 20 nm/60 nm Ti/Au using electron gun evaporator.
        NOTE: Gold is used to avoid the oxidization of the metal pads.
    3. Prepare and submerge the sample to 100 mL of acetone to dissolve PR and perform lift-off. Shake and blow the acetone while monitoring the whole process via optical microscopy until the metal pads become apparent.

7. Perform another EBL process to overlay a ribbon shape pattern on top of the MoS_2-WSe_2 heterojunction.
    1. Measure the coordinate displacement between the target locations in the MoS_2-WSe_2 heterojunction and the alignment marks using optical microscopy and design the ribbon-shape layout based on these measurements using a software (AutoCAD).
    2. Spin-coat PR, for example PMMA or P015, on top of the sample at 2000 rpm for 60 s (room temperature). Ensure that the PR has covered the entire sample after spin coating.
    3. Heat the sample (Soft Bake) at 100 °C for 90 s in order to evaporate the solvents in the PR and enhance the adhesion.
    4. Convert the pattern layout in step 1.7.1 into a specific file (example: GDS file), and upload it in the EBL software.
    5. Determine the ideal dose of electron beam based on the width of the lines in the layout.
        NOTE: For line width narrower than 1 µm, the ideal dose of electron beam is 110 µC/cm^2; for 1 to 5 µm line width, the dose is 100 µC/cm^2; and for line width wider than 5 µm, the dose is 80 µC/cm^2.
    6. Set up the EBL machine such that the position of the alignment marks in the sapphire substrate matches its correspondence in the layout.

7. Start exposing the sample to electron beam.
8. Apply PEB on the sample after exposure in order to reduce the standing wave effects. Heat the sample at 120 °C for 90 s.
9. Use TMAH 2.38% as the developer. Immerse the sample to TMAH for 80 s. Wash out the TMAH with 200 mL deionized water for 10 s.
10. Examine if the pattern is well developed by optical microscopy.
11. Conduct hard bake to get rid of extra water in PR. Heat the sample at 110 °C for 90 s.

8. Use O_2 plasma etching (2nd etching) to define a ribbon-shaped lateral heterojunction, and remove PR by acetone.
9. Perform the EBL process to overlay the pattern of the Ti/Au metal electrodes.
    1. Measure the coordinate displacement between the target locations in the MoS_2-WSe_2 heterojunction and the alignment marks using optical microscopy and design the metal electrode layout based on these measurements using a software (AutoCAD).
    2. Spin-coat PR, for example PMMA or P015, on top of the sample at 2000 rpm for 60 s (room temperature). Ensure that the PR has covered the entire sample after spin coating.
    3. Heat the sample (Soft Bake) at 100 °C for 90 s in order to evaporate the solvents in the PR and enhance the adhesion.
    4. Convert the pattern layout in step 1.9.1 into a specific file (example: GDS file), and upload it in the EBL software.
    5. Determine the ideal dose of electron beam based on the width of the metal lines in the layout.
    NOTE: For metal line width narrower than 1 μm, the ideal dose of electron beam is 110 μC/cm^2; for 1 to 5 μm line width, the dose is 100 μC/cm^2; and for line width wider than 5 μm, the dose is 80 μC/cm^2.
    6. Set up the EBL machine such that the positions of the alignment marks in the sapphire substrate matches its correspondence in the layout.
    7. Start exposing the sample to electron beam.
    8. Apply PEB on the sample after exposure in order to reduce the standing wave effects. Heat the sample at 120 °C for 90 s.
    9. Use TMAH 2.38% as the developer. Immerse the sample to TMAH for 80 s. Wash out the TMAH with 200 mL deionized water for 10 s.
    10. Examine if the pattern is well developed by optical microscopy.
    11. Conduct hard bake to get rid of extra water in PR. Heat the sample at 110 °C for 90 s.

10. Perform Ti/Au Metal Deposition and Lift-off
    1. Deposit Ti/Au metal using electron gun evaporator with the thickness of less than 100 nm, otherwise, it will be difficult to remove the PR and the unwanted metal by lift-off.
    2. Prepare and submerge the sample to 100 mL of acetone to dissolve PR and perform lift-off. Shake and blow the acetone while monitoring the whole process via optical microscopy until there are only metal lines and pads left.

11. Perform the EBL process in step 1.9 but overlay the Pd/Au metal electrode's pattern instead of Ti/Au.
12. Perform the metal deposition and lift-off process in step 1.10 but deposit Pd/Au instead of Ti/Au.

2. 2D Back-gated Transistors Fabrication Process

1. Prepare back-gated Si/SiO_2 substrates with alignment marks.
    1. Prepare homemade or commercial SiO_2/Si substrate.
    2. Use photolithography or EBL patterning techniques to define the alignment mark.
    3. Perform reactive ion etching (RIE) on the SiO_2/Si substrate until the total depth of the target area reaches 1000 nm and remove the PR by O_2 plasma to reveal the formed alignment marks.
    4. Overlay the patterns of metal pad arrays using photolithography patterning technique.
    5. Deposit 20 nm/60 nm Ti/Au using electron gun evaporator.
    NOTE: Gold is used to avoid oxidization of the metal pads.
    6. Prepare and submerge the sample to 100 mL of acetone to dissolve PR and perform lift-off. Shake and blow the acetone while monitoring the whole process by optical microscopy until the metal pads become apparent.

2. Perform CVD of MoS_2 on sapphire substrate in a hot-wall furnace.
    1. Place 0.6 g of MoO_3 powder in a quartz boat located at the heating zone center of the furnace. Put the sapphire substrate downstream next to the quartz boat containing the MoO_3 powder.
    2. Prepare S powder in a separate quartz boat at the upstream side of the furnace. Maintain its temperature at 190 °C during the reaction.
    3. Use argon (Ar = 70 sccm, 40 Torr) gas flow to bring the S and MoO_3 vapors to the sapphire substrate while heating the center zone to 750 °C.
    4. Keep the heating zone, after reaching the desired growth temperature of 750 °C, for 15 min and then naturally cool down the furnace to room temperature.

3. Transfer MoS_2 from the sapphire to the back-gated SiO_2/Si substrate.
    1. Spin coat PMMA with the spin speed of 3500 rpm for 30 s on top of the MoS_2 film.
    2. Bake the MoS_2/sapphire sample at 120 °C for 3 min in order to strengthen the PMMA coating.
    3. Dip the MoS_2/Sapphire sample into 50 mL of ammonia solution (14.5%) for around 30 min to 2 h to separate the MoS_2 film from the sapphire substrate.
    4. Pick up the film and transfer it to the SiO_2/Si substrate.
    5. Bake the MoS_2/SiO_2/Si sample in order to enhance the adhesion between the MoS_2 and SiO_2 layers. Heat the sample at 120 °C for around 30 min to 1 h.
    6. Remove the PMMA by washing it with 30 mL of acetone for around 30 min to 2 h.
    7. Rinse the sample with isopropyl alcohol and use nitrogen to blow it dry.

4. Perform EBL.
NOTE: There is no thin Au deposited on SiO_2/Si substrate during EBL process since Si is somehow conductive.

1. Measure the coordinate displacement between the target locations and the alignment marks using optical microscopy and, based on these measurements, design the pattern layout of the metal electrodes using a design software.
   NOTE: Metal electrodes connect the target points in the MoS_2 sample to the metal pads in the SiO_2/Si substrate.
2. Spin-coat PR, for example PMMA or P015, on top of the sample at 2000 rpm for 60 s (room temperature). Ensure that the PR has covered the entire sample.
3. Heat the sample (Soft Bake) at 100 °C for 90 s in order to evaporate the solvents in the PR and enhance the adhesion.
4. Convert the pattern layout in step 2.4.1 into a specific file (example: GDS file), and upload it in the EBL software.
5. Determine the ideal dose of electron beam based on the width of the metal lines in the layout.
   NOTE: For metal line width narrower than 1 µm, the ideal dose of electron beam is 110 µC/cm^2; for 1 to 5 µm line width, the dose is 100 µC/cm^2; and for line width wider than 5 µm, the dose is 80 µC/cm^2.
6. Set up the EBL machine such that the position of the alignment marks in the Si/SiO_2 substrate matches its correspondence in the layout.
7. Start exposing the sample to electron beam.
8. Apply PEB on the sample after the exposure in order to reduce the standing wave effects. Heat the sample at 120 °C for 90 s.
9. Use TMAH 2.38% as the developer. Immerse the sample to TMAH for 80 s. Wash out the TMAH with 200 mL of deionized water for 10 s.
10. Examine if the pattern is well developed by optical microscopy.
11. Conduct hard bake to get rid of extra water in PR. Heat the sample at 110 °C for 90 s.

5. Perform Au Metal Deposition and Lift-off
   1. Deposit Au metal using electron gun evaporator with the thickness of less than 100 nm, otherwise, it will be difficult to remove the PR and the unwanted metal by lift-off.
   2. Prepare and submerge the sample to 100 mL of acetone to dissolve PR and perform lift-off. Shake and blow the acetone while monitoring the process via optical microscopy until there are only metal lines and pads left.

Representative Results

The device fabrication processes have been applied to several of the corresponding author's researches involving the development of 2D material devices. In this part, the results of some of these researches are presented to demonstrate the effectivity of the protocol discussed above. A monolayer of lateral WSe_2-MoS_2 Q-HBT[20] is selected as the first example. Using the standard device fabrication processes detailed in the protocol, the monolayer lateral WSe_2-MoS_2 heterojunctions were grown (**Figure 2a**) and then proceeded by the formation of the Q-HBT. Metal contacts were deposited on top of the lateral heterojunction to complete the Q-HBT. Ti/Au were deposited on top of the MoS_2 layer (**Figure 2c**), followed by the deposition of Pd/Au on top of the WSe_2 layer (**Figure 2d**). Several lateral Q-HBT were developed, such as the one with an n-p-n-p lateral heterojunction illustrated in (**Figure 2d**, **2e**). The function of the Q-HBT device was verified by looking into its characteristic curves such as its output (I_C-V_{CE}) curve at common-emitter configuration (**Figure 2f**). **Figure 2f** shows that the lateral n-p-n Q-HBT works under two operating modes - the saturation mode and the active mode - which proves that the Q-HBT that was built using the fabrication process, indeed, functions as a transistor.

The process was also used to build 2D back-gated devices for MoS_2 piezotronic strain/force sensor[21] application. High-quality triangular monolayer MoS_2 films were first synthesized using CVD in a sapphire substrate and then transferred into a Si/SiO_2 substrate. The rest of the process of making the MoS_2 film into a piezotronic device is discussed in the protocol section. **Figure 3a** shows an atomic force microscopy (AFM) image of a completed device consisting of a triangular MoS_2 monolayer and several sets of source/drain (S-D) Au electrodes. To study the piezoelectric polarization direction, multiple contact electrodes around the triangle shape were intentionally designed. **Figure 3b** presents the schematic diagram of the piezotronic sensor device and the setup showing how a mechanical load is applied by an AFM tip to test its piezoelectric effect. Results in **Figure 3c** show that the sensor device's current flowing through one of its S-D electrode pairs decreases for every increase in applied force and vice versa, which is an expected behavior for a piezo sensor. Furthermore, the data in **Figure 3d** implies that the developed sensor is stable since a repeating application of applied force/strain barely changed its output current or response.

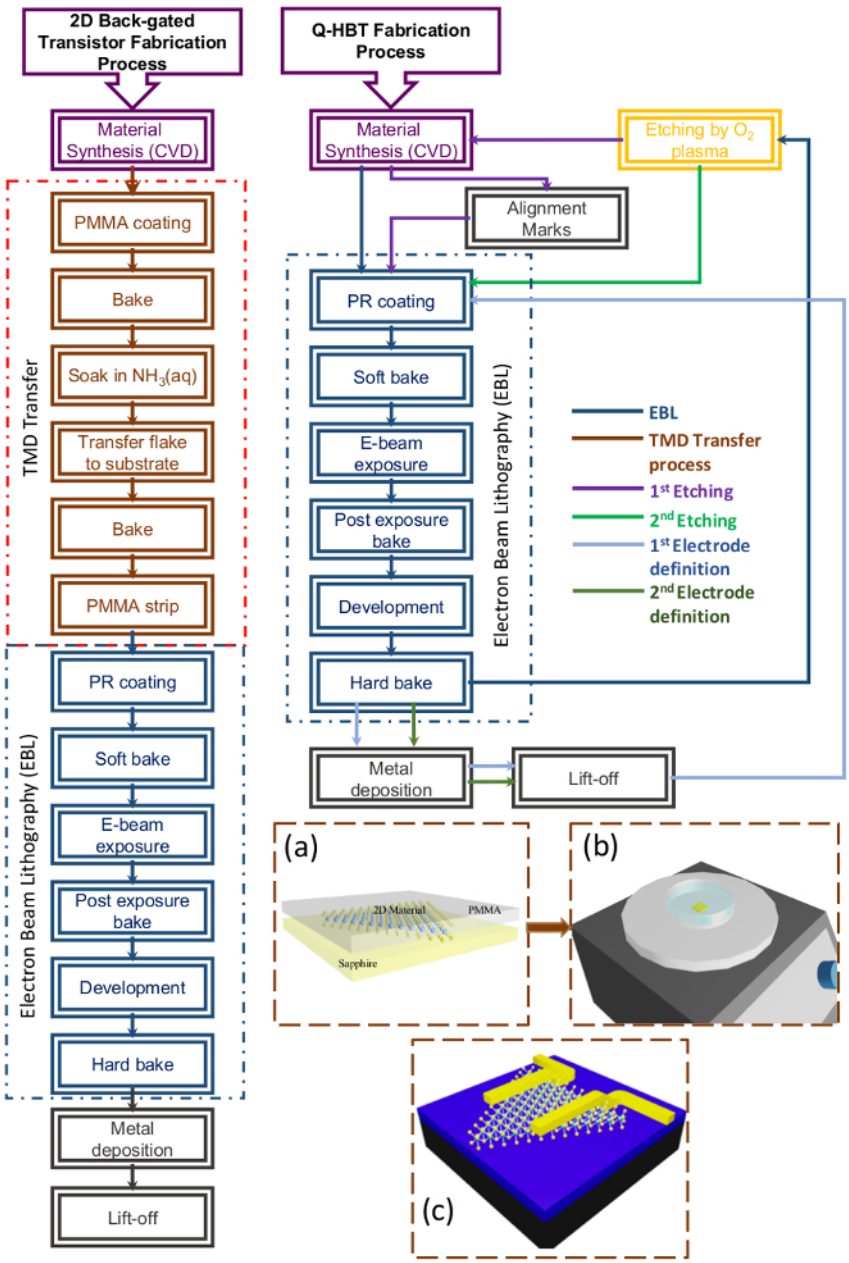

Figure 1. Schematic process flow of 2D electronic devices. The blue arrows represent the fabrication process flow of Q-HBT and brown for 2D back-gated transistor. Inset: **(a)** the 2D material on sapphire substrate coated with PMMA; **(b)** a sample heated while soaked in ammonia solution; **(c)** schematic diagram of a 2D material after metal deposition and lift-off process. Please click here to view a larger version of this figure.

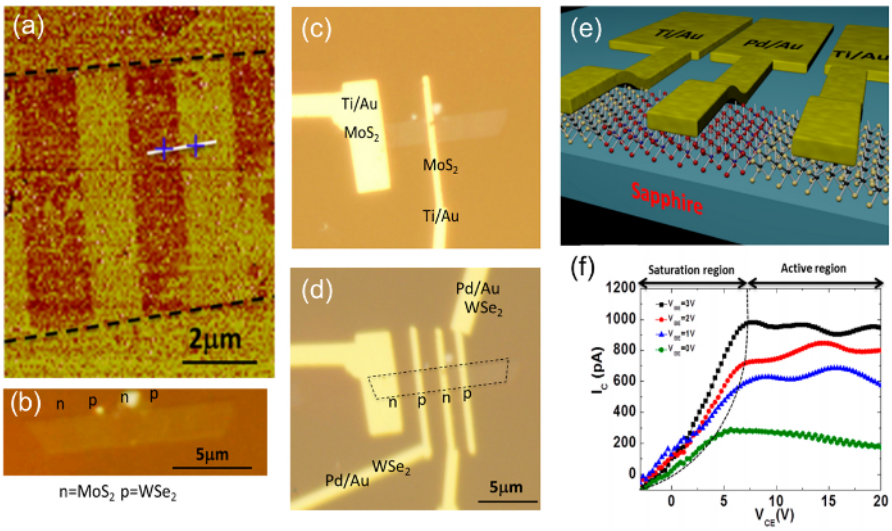

Figure 2. Two-dimensional lateral Q-HBT. (a). Phase image of AFM. The phase image shows clear contrast between WSe_2 and MoS_2. **(b).** The optical micrograph of a lateral heterostructure ribbon where n-type material is MoS_2 and p-type material is WSe_2. **(c).** The optical micrograph of the metal Ti/Au deposited on top of MoS_2 in the lateral heterostructure ribbon. Note that this image has the same scale as in (d). **(d).** The optical micrograph of the lateral Q-HBT, showing an n−p−n−p lateral heterojunction. Black dashed box marks the position of the lateral heterostructure ribbon. **(e).** Schematic plot of a 2D Q-HBT. The yellow ribbons are MoS_2 monolayers and the red ribbon is WSe_2 monolayer. Ti/Au metal layers are designed to deposit on MoS_2 while Pd/Au contacts with WSe_2. **(f).** The output characteristics of the lateral n−p−n Q-HBT at different V_{BE} values. Reprinted with permission from Blaschke, B. M., *et al.*[10]. Please click here to view a larger version of this figure.

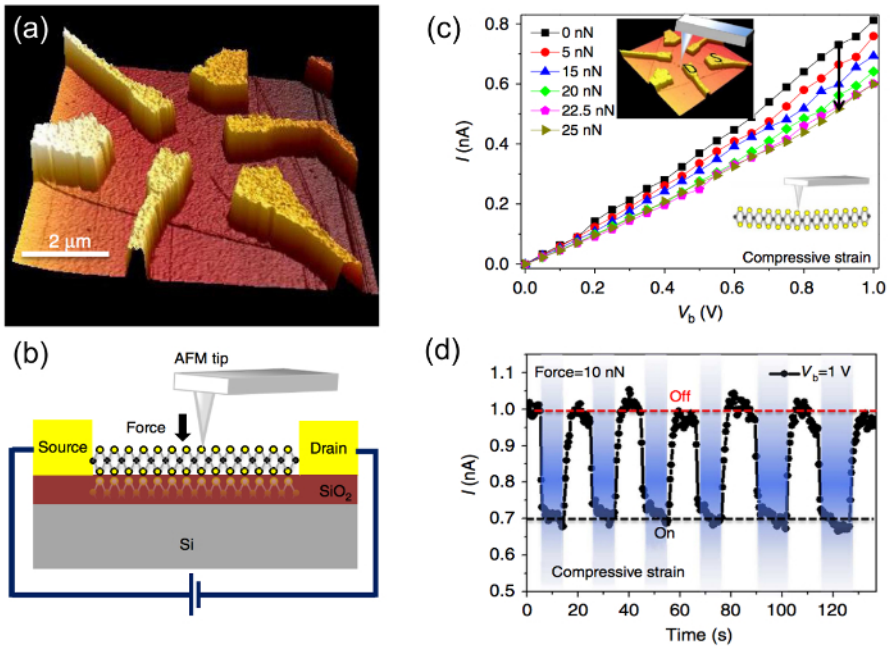

Figure 3. The MoS_2 monolayer device. (a). AFM image of the MoS_2 monolayer device. **(b).** Schematic illustration of a MoS_2 device showing how a mechanical load is applied by an AFM tip to test its piezoelectric effect. **(c).** I-V_b characteristics of the MoS_2 device at different applied forces under compressive strain when applying forces at locations denoted in upper inset resulting in compressive strain as shown schematically in lower insets. **(d).** Current response of CVD monolayer MoS_2 device at repeated compressive strains at a fixed bias voltage of 1 V. Reprinted with permission from Lan, Y. W., *et al.*[8]. Please click here to view a larger version of this figure.

Discussion

In this article, the detailed procedures of fabricating novel electronics based on 2D materials in nanometer scale are demonstrated. Since the sample preparation procedures of each application have differences with each other, the overlapped processes were treated as the protocol. Electron beam patterning combined with material location determination and metal electrode definition thus serves as the protocol here. Among the two types of devices mentioned, the whole process of 2D back-gated transistors starting at wet transferring single crystal MoS_2 films onto SiO_2/Si substrates and ending at metal lift-off were presented. The reason why focus is given on 2D back gated transistors is the urgent need of

improved 2D materials-based field effect transistors (FETs). Therefore, important points related to its fabrication process will be emphasized in the following paragraphs.

There are some tricky points in every step of the experiments. Firstly, the precedence of material locating followed by the removal of PMMA is required to avoid unfavorable adsorption while exposing the MoS_2 films to air. The adsorption is one of the causes of performance degradation. Consequently, baking the sample, with a duration that is supposed to be longer than 30 min, after the transfer is necessary. Otherwise, the film is easy to be peeled off when dissolving PMMA with acetone due to the poor attachment of the films and dielectric, which results in the disappearance of the flakes at target positions. The dose of electron beam is another critical factor for patterning. High electron beam dosage is not suitable for patterns with narrow spacing between electrodes due to the proximity effect. On the other hand, decreasing its dosage may lead to the inability to achieve the ideal pattern. Fine tuning of the parameters of electron beam therefore needs to be conducted. Basically, a thin metal is preferable for easier lift-off, and its ideal thickness depends on the application and the thickness of the photo resist. For the 2D transistor in this project, metal thickness below 100 nm is acceptable.

One limitation of the method is that manual operation is required, so it is only suitable for research purposes. Once wafer scale synthesis techniques of these materials become well-developed, traditional semiconductor technology can take over this approach. Also, a trade-off between getting a higher resolution and material quality exists when choosing between optical imaging and the alternative method using scanning electron microscope (SEM) in determining the material location. The optical imaging method used in this protocol provides micrometer scale precision for locating positions, while SEM is more precise but could induce damage in the material. Therefore, using optical imaging as proposed in the protocol is the most expedient by far.

Since years of research seeking for the best way to develop new materials is indispensable, laboratory scope manufacturing with hands-on experiments still occupies an important position. Surely, this method can serve not only for 2D materials but also for 1D and the undiscovered materials in future, broadening the possibilities of nanoscale electronics.

Disclosures

The authors have nothing to disclose.

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