Video Article

Flow-assisted Dielectrophoresis: A Low Cost Method for the Fabrication of High Performance Solution-processable Nanowire Devices

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Abstract

Flow-assisted dielectrophoresis (DEP) is an efficient self-assembly method for the controllable and reproducible positioning, alignment, and selection of nanowires. DEP is used for nanowire analysis, characterization, and for solution-based fabrication of semiconducting devices. The method works by applying an alternating electric field between metallic electrodes. The nanowire formulation is then dropped onto the electrodes which are on an inclined surface to create a flow of the formulation using gravity. The nanowires then align along the gradient of the electric field and in the direction of the liquid flow. The frequency of the field can be adjusted to select nanowires with superior conductivity and lower trap density.

In this work, flow-assisted DEP is used to create nanowire field effect transistors. Flow-assisted DEP has several advantages: it allows selection of nanowire electrical properties; control of nanowire length; placement of nanowires in specific areas; control of orientation of nanowires; and control of nanowire density in the device.

The technique can be expanded to many other applications such as gas sensors and microwave switches. The technique is efficient, quick, reproducible, and it uses a minimal amount of dilute solution making it ideal for the testing of novel nanomaterials. Wafer scale assembly of nanowire devices can also be achieved using this technique, allowing large numbers of samples for testing and large-area electronic applications.

Video Link

The video component of this article can be found at https://www.jove.com/video/56408/

Introduction

Controllable and reproducible assembly of nanoparticles in pre-defined substrate locations is one of the main challenges in solution-processed electronic and photonic devices utilizing semiconducting or conducting nanoparticles. For high performance devices, it is also highly beneficial to be able to select nanoparticles with preferential sizes, and particular electronic properties, including, for example, high conductivity and low density of surface trap states. Despite significant progress in nanomaterials growth, including nanowire and nanotube materials, some variations of nanoparticle properties are always present, and a selection step can significantly improve nanoparticle-based device performance[1,2].

The purpose of the flow-assisted DEP method demonstrated in this work is to address the above challenges by showing controllable semiconducting nanowires assembly onto metallic contacts for high performance nanowire field effect transistors. DEP solves several problems of nanowire device fabrication in a single step including positioning of nanowires, alignment/orientation of nanowires, and selection of nanowires with desired properties *via* DEP signal frequency selection[1]. DEP has been used for numerous other devices ranging from gas sensors[3], transistors[1], and RF switches[4,5], to the positioning of bacteria for analysis[7].

DEP is the manipulation of polarizable particles via the application of a non-uniform electric field resulting in nanowires self-assembly across the electrodes[8]. The method was originally developed for the manipulation of bacteria[9,10] but has since been expanded to the manipulation of nanowires and nanomaterials.

DEP solution processing of nanoparticles enables semiconductor device fabrication that significantly differs from traditional top-down techniques based on multiple photomasking, ion implantation, high temperature[14], annealing, and etching steps. Since DEP manipulates nanoparticles that have already been synthesized, it is a low-temperature, bottom-up fabrication technique[11]. This approach allows large-scale nanowire devices to be assembled on almost any substrate including temperature-sensitive, flexible plastic substrates[6,12,13].

In this work, high performance p-type silicon nanowire field effect transistors are fabricated using flow-assisted DEP, and the FET current-voltage characterization is conducted. The silicon nanowires used in this work are grown via the Super Fluid Liquid Solid (SFLS) method[15,16]. The nanowires are intentionally doped, and are approximately 10 - 50 µm in length and 30 - 40 nm in diameter. The SFLS growth method

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is very attractive since it can offer industry scalable amounts of nanowire materials[15]. The proposed nanowire assembly methodology is directly applicable to other semiconductor nanowire materials such as InAs[13], SnO_2[3], and GaN[18]. The technique can also be expanded to align conductive nanowires[19] and to position nanoparticles across electrode gaps[20].

Protocol

Caution: All procedures unless otherwise stated take place in a clean room environment and risk assessments have been done to ensure safety during nanowires and chemicals handling. Nanomaterials may have a number of health implications which are as of yet unknown, and so should be handled with appropriate care[21].

NOTE: The process starts with the preparation of the substrates, followed by the first photolithography and metal deposition steps to define the DEP contacts. The nanowires are then assembled via DEP and a further optional photolithographic and metal deposition step can be performed to deposit top contacts onto nanowires. The nanowire transistor devices current-voltage characteristics are then measured using a semiconductor characterization kit.

1. Preparation of Substrates

1. Cut a doped n-type silicon/silicon dioxide wafer into suitable sizes, *e.g.*, 2.5 cm^2.
2. During cutting, ensure the top surface of the wafer is not touched or scratched.
3. Run a diamond scriber across the surface in one continuous motion to make a cut.
4. Split the wafer along the cut.
5. Place the samples on a substrate holder and sonicate for 5 min in an ultra-sonic bath at 100% power (450 W), first in deionized water, then acetone, and finally isopropanol (IPA).
   NOTE: See **Table of Materials** for CAS numbers and suppliers.
6. Dry the substrates with a nitrogen gun to remove any remaining IPA or dust from the surface.
7. Plasma ash the samples in oxygen plasma at 100 W for 5 min to remove any remaining organic residues.

2. Photolithography Bilayer Process for Contacts

NOTE: A bilayer photolithography process is used to create electrodes. The photolithography process is conducted in a yellow room to prevent decay of photoresist materials.

1. Heat the sample at 150 °C for 15 min using a hotplate, to remove any remaining water from the surface.
   NOTE: This is to ensure adhesion of photoresist; however chemical primers such as HMDS may also be used.
2. Remove the sample from the hot plate and place it on a spin-coater.
3. Using a pipette, drop approximately 1 mL of photoresist A on the surface until the entire sample is uniformly covered.
   NOTE: See **Table of Materials** for the exact photoresist used.
4. Spin the sample at 4,000 rpm for 45 s, to produce a film thickness of approximately 250 nm. If electrodes that are thicker than 150 nm are to be deposited, change this recipe.
5. Remove the sample from the spin-coater and place it on a hotplate at 150 °C for 5 min.
6. Remove the sample from the hotplate and leave the sample to rest for 5 min in a 50% humidity box. This is to ensure rehydration of the photoresist[22].
   NOTE: If the humidity of the lab is greater than 50%, the sample may be left to rest in the air.
7. Place the sample back onto the spin-coater and pipette approximately 1 mL of photoresist B on the surface of the substrate.
8. Spin the sample at 3,500 rpm for 45 s, giving a film thickness of approximately 500 nm.
9. Place the sample on a hotplate at 120 °C for 2 min.
10. Remove the sample from the hotplate and leave to rest in a 50% humidity box for 5 min.
11. Expose the sample using a mask-aligner and photomask to UV light for 6.7 s for a total of 180 mJ of exposure.
    NOTE: The exact exposure dose might need to be adjusted depending on a particular model of mask aligner.
12. Remove the sample from the mask-aligner and develop by immersing it in photoresist developer for 30 s.
    NOTE: See **Table of Materials** for the exact developer.
13. Remove the sample from the developer, immerse the sample into deionized water, and rinse it to stop the development process.
14. Check the photolithography using an optical microscope. A polarizer can be used to check the bilayer undercut which should appear as faint lines around the channel. The time may be adjusted if too much or two little undercut is achieved.

3. Deposition of Metal Contacts

NOTE: Electron beam (E-beam) deposition is used to deposit electrodes onto the prepared photoresist. This process can also use thermal evaporators or other types of metal thin film deposition techniques.

1. Place the samples in the E-beam chamber; pump it down until a high vacuum is reached. In this case, a vacuum of around 1 x 10^{-6} mTorr is reached.
2. Deposit 2 - 6 nm of titanium which acts as an adhesion layer followed by 30 nm of gold for the DEP contacts.
3. Remove the samples from the E-beam chamber.
4. Perform the lift-off procedure by removing most of the photoresist and excess metal. This is done by placing the samples into a beaker of photoresist remover for 15 min.
5. Remove the samples from the beaker of photoresist remover A and place into another clean beaker of photoresist remover for a further 15 min. This is to prevent any large metal particles from settling on the sample.

6. Complete lift-off by sonicating the beaker for 5 min at 50% power.
7. Remove the samples from the bath one-by-one, ensuring to rinse off any material with IPA to prevent undesired metal particles from settling between electrodes.
   NOTE: The electrodes are now prepared for the DEP alignment of nanowires.

4. DEP of Nanowires

1. Prepare a solution of silicon or other nanowires in anisole of approximately 1 µg/mL concentration. In this experiment, the solution is briefly sonicated for 15 s at the lowest power setting possible to remove any flocculation. Other solvents can be used such as toluene and N,N-dimethylformamide (DMF)[1].
2. Check the solution by drop casting a 10 µL of the nanowire formulation onto a sacrificial substrate.
3. Inspect the substrate with deposited nanowires using a polarized optical microscope (POM). The silicon nanowires are birefringent and hence can be easily seen in POM. If there are no nanowire clumps visible, and most of nanowires are well dispersed on the substrate, then the next stage can begin, otherwise the solution is re-sonicated, and the nanowire concentration might need to be adjusted. It may take several attempts to achieve the correct nanowire dispersion.
4. Place the prepared sample with electrodes onto 30° (vs. horizon) inclined platform with the device channel aligned horizontally. The dispersion flow direction needs to be perpendicular to the electrodes edges to allow more efficient nanowire alignment.
5. Contact the electrodes using micro-probes connected to a frequency generator[1].
6. Set the desired frequency and voltage are on the frequency generator. In this experiment, use a DEP signal voltage of 10 V peak-to-peak and a 1 MHz sinewave.
   NOTE: Increasing the frequency up to 20 MHz can help to collect nanowires with high conductivity and low trap density[1,2]. See reference[1] for a detailed discussion. DEP signal frequency range indicated here was obtained by conducting SFLS Si nanowires impedance spectroscopy and collection time analysis, as described in reference[1]. Other types of nanowires with higher or lower charge carrier mobility, doped nanowires, or nanowires obtained by other growth methods can have different DEP signal frequency range resulting in the collection of high quality nanowires.
7. Switch-on the frequency generator and drop approximately 10 µL of nanowire solution using a micropipette onto the device area.
   NOTE: Placing the sample at an angle (30°) helps to create a gravity-assisted slow flow of the liquid. Alternatively, a capillary action using a glass slide can be used[6].
8. Apply the DEP signal for 30 s and then switch-off the frequency generator.
9. Remove the sample and rinse very gently with IPA.
10. Dry-off the sample very gently using a nitrogen gun. A polarized optical microscope may be used to inspect the sample and adjust parameters
    NOTE: The DEP signal voltage, frequency, and the nanowire dispersion density can be adjusted to achieve a reproducible desired density of nanowires, from a few nanowires to a few hundred per device[1,2].

5. Deposition of a Secondary Metal Layer

1. To achieve improved current injection in NW FETs, apply a second metallic contact on top of the nanowire.
   NOTE: This contact deposition process follows the exact same steps as sections 2 and 3, in both photolithography and metal deposition, except that only a gold layer is deposited.

6. I-V Characterization of Nanowire Devices

NOTE: The samples are now complete and can be used in subsequent experiments or their I-V characteristics can be measured to establish nanowire FET electrical properties. The fabricated devices are back-gated FETs, where doped silicon wafer serves as the common gate, and SiO_2 layer serves as the gate dielectric.

1. To establish electrical contact with the gate, remove a small area of the silicon oxide at the edge of the sample using a diamond scriber.
2. Use a nitrogen gun to remove any undesired silicon dioxide particles.
3. Place three microprobes (source, drain, and gate) on the gold source-drain electrode contacts, with the gate probe on the area with removed SiO_2.
4. Use a semiconductor characterization system to take I-V measurements.
5. Measure transfer and output scans of NW FETs as these give information on the performance of the device and the electrical properties of the nanowires[1,17,23]. Note that transfer measurements involve stepping source-drain voltage and sweeping gate voltage. The output characteristics are measured by sweeping source-drain voltage and stepping gate voltage.

Representative Results

Bilayer photolithography results in clean sharply defined electrodes. In the example (**Figure 1A**), inter-digitated finger structure was used with a channel length of 10 µm. These structures allow a large area to assemble the maximum number of nanowires when the DEP force is applied. **Figure 1B** shows a schematic of a bottom-gate nanowire FET device.

Incorrect nanowire dispersion concentration, as well as insufficient sonication can result in poor quality dispersions, with drop cast examples of nanowires shown in **Figure 2A** and **Figure 2B**, with a significant amount of nanowire clumps. DEP deposition of very dense nanowire dispersions can also produce undesirable quality layers of nanowires as shown in **Figure 2C**. In this example, nanowires are deposited too densely, resulting in a very significant nanowire-nanowire screening effect. An example of good DEP deposition is shown in **Figure 2D**, demonstrating well-dispersed, isolated, aligned nanowires.

Flow-assisted DEP of nanowires should result in nanowires perpendicularly crossing the channel with an overlap of several microns onto the electrode as shown in **Figure 3**. Ideal nanowire assembly can be approximated as a well-aligned "monolayer". Additionally, a small gap between the nanowires is preferred to reduce the nanowire screening effect. An example of controllable nanowire assembly by flow assisted DEP is shown in **Figure 3A** and **Figure 3B**, where DEP signal voltage was reduced in **Figure 3B**, resulting in a significantly smaller number of nanowires deposited in the electrode gap.

Transfer and output scans of a typical silicon nanowire field effect transistor are shown in **Figure 4**. The results demonstrate that the device has p-type behavior, with well-defined gate modulation. These results compare well with other nanowire transistors fabricated using the same method in the literature[1,2]; however, these devices can also be improved by techniques such as surface passivation which is not discussed here[17]. Solution processed silicon nanowire FETs have exhibited on currents as high at milliamp level[1]; however, for many applications, FETs with micro-amp currents are sufficient.

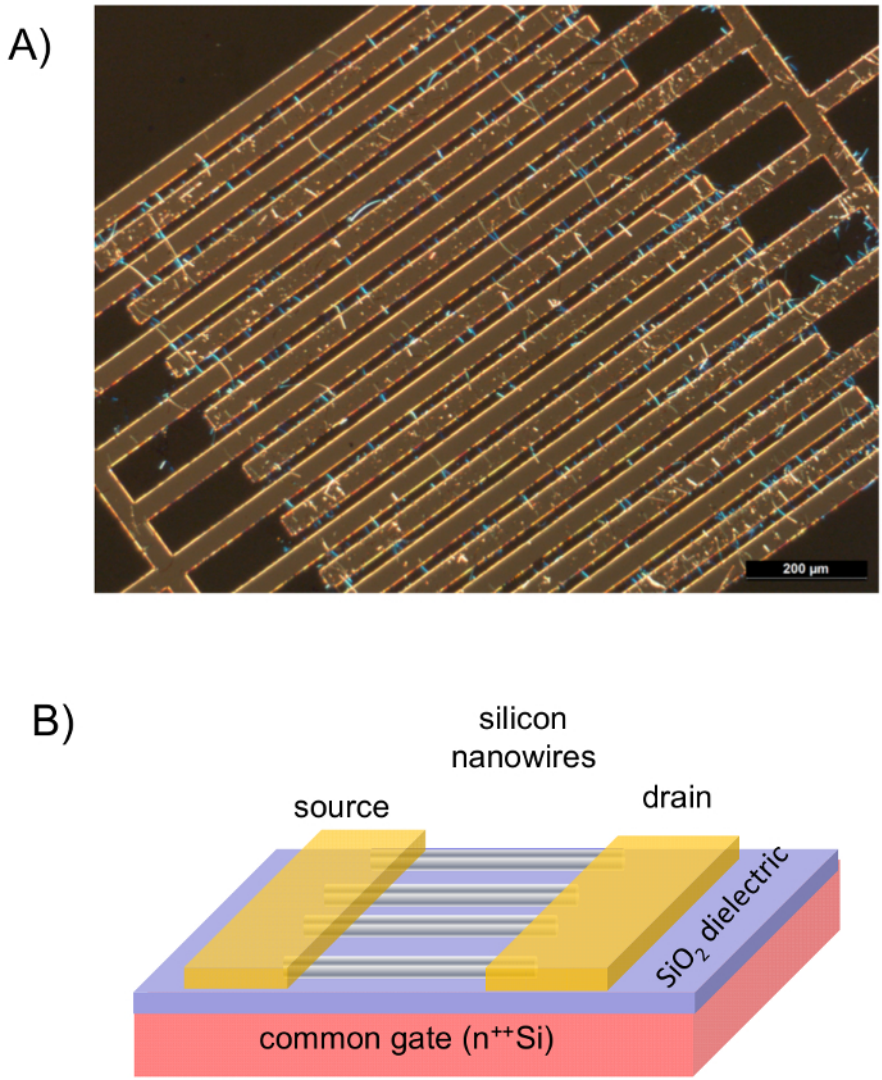

Figure 1: Optical image and schematic of the transistor. (**A**) Optical microscope image of interdigitated electrode structures with nanowires aligned between the electrodes. (**B**) Schematic of a bottom-gate nanowire field-effect transistor built on Si/SiO_2 wafer with Si common gate. Please click here to view a larger version of this figure.

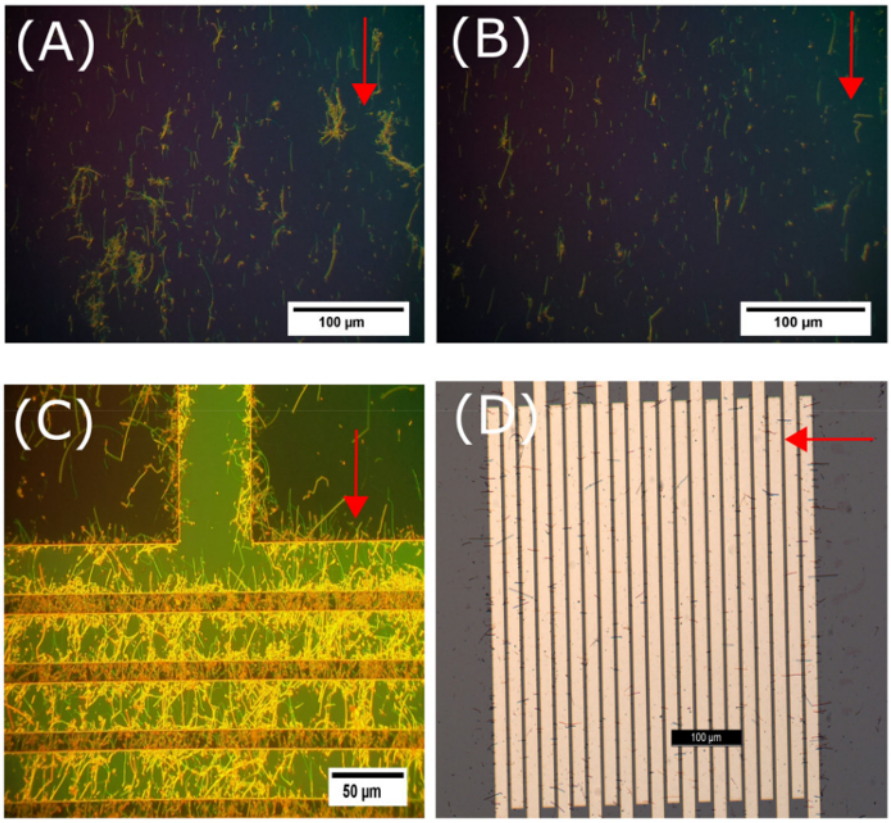

Figure 2: Polarized optical microscope images of solution deposit silicon nanowires. (**A**) Example of nanowires drop cast on silicon wafers from an unoptimized dispersion, showing a significant number of nanowire clumps. (**B**) Drop cast nanowires after brief sonication with fewer clumps. (**C**) Device after incorrect DEP showing a very high density of nanowires, and clumps. (**D**) Device after correct DEP deposition showing well-aligned, isolated nanowires crossing the electrode gaps. Red arrows indicate the direction of fluid flow. Please click here to view a larger version of this figure.

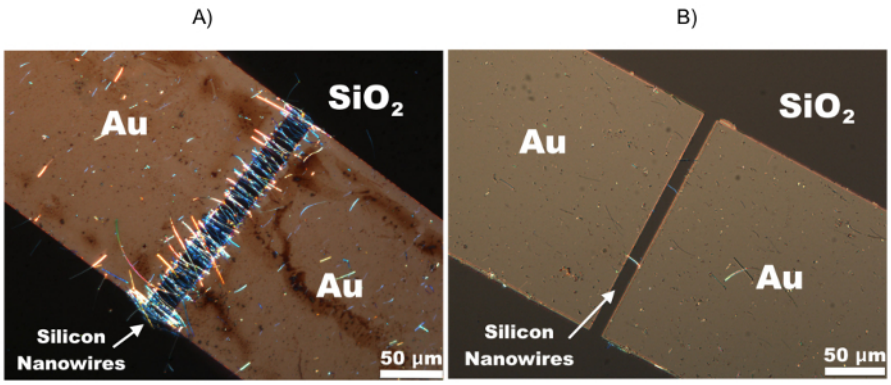

Figure 3: Polarized optical microscope images of controllable DEP deposition of silicon nanowires. (**A**) Nanowires assembled at high DEP signal voltage (15 V), showing high density of aligned nanowires. (**B**) Nanowires assembled at low DEP voltage (5 V), with only two nanowires bridging the electrodes. Please click here to view a larger version of this figure.

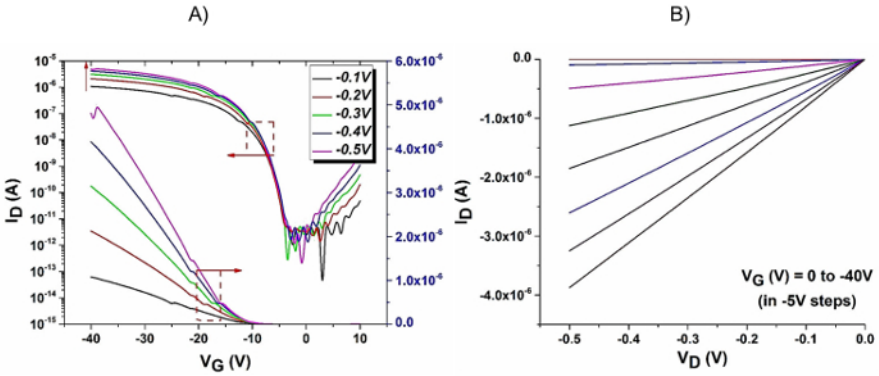

Figure 4: Typical nanowire FET device I-V characteristics. (**A**) FET transfer scan of a silicon nanowire bottom gated FET device with gold electrodes. Drain voltages are stepped from -0.1 to -0.5 V with -0.1 V interval and gate voltage is swept from 10 to -40 V. (**B**) Output scan of the same device with stepped gate voltage from 0 to -40 V with -5 V intervals and swept drain voltage from 0 to -0.5 V. Nanowires were assembled at DEP signal at 2 MHz and 10 Vpp. FET demonstrates 5 pA off-current (V_G = 0 V), 5 µA on-current at V_D= 0.5 V, resulting in 10^6 - 10^7 on/off current ratio. Please click here to view a larger version of this figure.

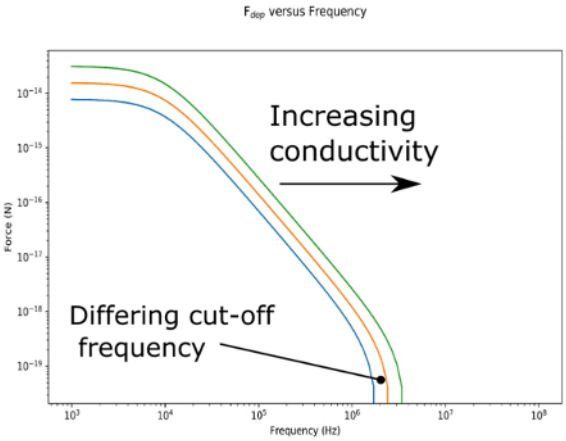

Figure 5: Simulated plot of DEP force versus frequency for silicon nanowires in anisole with differing conductivities. In the simulation, the nanowires have a permittivity of 11.9 and a conductivity of between 2.5 x 10^{-2} S/m to 10 x 10^{-2} S/m. Anisole has a permittivity of 4.33 and an assumed conductivity of 2 x 10^{-6} S/m. Note that higher conductivities have a higher frequency at which the force drops to zero. This trend indicates that higher conductivity nanowires can be collected at higher DEP signal frequency. Please click here to view a larger version of this figure.

Discussion

The successful fabrication and performance of the devices depend on several key factors. These include nanowire density and distribution in the formulation, the choice of solvent, the frequency of DEP, and the control of the number of nanowires present on the device electrodes[1].

One of the critical steps in achieving repeatable working devices is the preparation of a nanowire formulation without clusters or clumps. The formulation can be sonicated before DEP to reduce the number of clumps and to maintain nanowire dispersion. Density of a solution once made can also be difficult to control especially if nanowires are likely to coagulate which can lead to a less dense formulation. Surfactants may be used to create a more disperse formulation, however the surfactant may have a negative effect of the device performance.

Figure 2A shows an example of drop cast deposited nanowires, with a significant number of clumps. If the clumps of nanowires are difficult to remove or the nanowires are susceptible to breaking during sonication[16], it is recommended that the solution be allowed to settle for a few seconds. The top of the formulation should then be pipetted off for use. Well-dispersed nanowires float on top of the solution, whereas heavy nanowire clusters sink to the bottom.

The choice of solvent and nanomaterial will affect the parameters in the DEP deposition stage. The dielectrophoretic force that a nanowire experiences is given by **Equation 1**[8]**:**

$$F_{DEP} = \Gamma \, \mathbb{R}[K(\omega)] \nabla |E^2| \quad (1)$$

where Γ is a geometry factor which is related to radius and length of the nanowire, $\nabla |E^2|$ is gradient of the root mean square of the electric field, and $\mathbb{R}[K(\omega)]$ is the real part of the Clausius-Mossotti factor (**Equation 2**).

$$K(\omega) = \frac{\varepsilon_p - \varepsilon_m - j(\sigma_p - \sigma_m)/\omega}{\varepsilon_p + 2\varepsilon_m - j(\sigma_p + 2\sigma_m)/\omega} \quad (2)$$

where ε_p and ε_m are the particle and medium permittivity's, σ_p and σ_m are their conductivity's, and ω is the frequency of DEP. From **Equation 2**, the force is dependent upon the conductivity and permittivity of both the solvent and the nanomaterial. If the solvent is changed, this may significantly alter the frequency and force response for the nanowires assembly. It is also evident that different nanowire materials will respond differently even in the same solvent.

$K(\omega)$ indicates that, at different frequencies, the particle may be more or less polarizable than the medium, which in turn determines whether the nanowires move toward the region of high electric field gradient (positive DEP) or toward the region of low electric field gradient (negative DEP)[1].

Figure 5 shows a simulated curve of the force experienced by silicon nanowires in anisole. The nanowires are assumed to have a permittivity of 11.9 and a conductivity of 2.5 x 10^{-2} to 5 x 10^{-2} S/m. Anisole has a permittivity of 4.33 and an assumed conductivity of 2 x 10^{-6} S/m. The frequency at which the force drops to zero is different for different conductivities. The effect may be used to select different particles based of their relative conductivity and permittivity by altering the applied frequency[1,2,24]. Higher frequencies have been found to select nanowires with higher conductivity and a lower density of traps. This selection leads to FET devices with significantly increased on-current per nanowire and improved sub-threshold slope[1].

This effect depends on the type of electrodes used and the angle of inclination of the substrate. We recommend for researchers wishing to adjust this process to their electrodes, to calibrate it by altering only one parameter at a time.

The number of nanowires present in the device channel area is also critical in achieving repeatable working devices, as too many nanowires will result in a mat as shown in **Figure 2C**, which can lead to poor I-V device characteristics, due to nanowires screening each other and reducing the effect of the gate field on the channel.

To control the density of nanowires, the voltage, frequency, and concentration of the formulation may be altered[1]. For example, to increase the number of nanowires, voltage may be increased, or concentration of the nanowire formulation increased. Frequency of the DEP signal is a very important parameter, as it has strong impact on the quality of the collected nanowires, so the reduction of frequency is not recommended, if high performance nanowire devices are to be prepared. It should also be noted that in some cases a high voltage may cause certain types of highly conducting nanowires to melt[19], or burn the contact areas.

In summary, DEP nanowire assembly is a very powerful technique, when coupled with impedance spectroscopy, allowing to evaluate DEP signal frequencies for the collection of high quality nanowires. At high DEP signal frequencies, in the 1 - 20 MHz range, identified for high quality Si nanowire collection, well-controllable and reproducible nanowire assembly can be obtained. In many cases, nanowire assembly of tens to a few hundred of nanowires per device area are sufficient for the demonstration of high performance nanowire transistors. The methodology is straightforward to extend to other types of nanowires and nanomaterials, if each material is examined in terms of its response to the DEP signal[1,2].

Disclosures

The authors confirm that there are no conflicts of interest.

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