

Video Article

# Fabrication of Low Temperature Carbon Nanotube Vertical Interconnects Compatible with Semiconductor Technology

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## Abstract

We demonstrate a method for the low temperature growth (350 °C) of vertically-aligned carbon nanotubes (CNT) bundles on electrically conductive thin-films. Due to the low growth temperature, the process allows integration with modern low-k dielectrics and some flexible substrates. The process is compatible with standard semiconductor fabrication, and a method for the fabrication of electrical 4-point probe test structures for vertical interconnect test structures is presented. Using scanning electron microscopy the morphology of the CNT bundles is investigated, which demonstrates vertical alignment of the CNT and can be used to tune the CNT growth time. With Raman spectroscopy the crystallinity of the CNT is investigated. It was found that the CNT have many defects, due to the low growth temperature. The electrical current-voltage measurements of the test vertical interconnects displays a linear response, indicating good ohmic contact was achieved between the CNT bundle and the top and bottom metal electrodes. The obtained resistivities of the CNT bundle are among the average values in the literature, while a record-low CNT growth temperature was used.

## Video Link

The video component of this article can be found at <https://www.jove.com/video/53260/>

## Introduction

Copper and tungsten, the metals which are currently used for the interconnects in state-of-the-art very-large-scale integration (VLSI) technology, are approaching their physical limits in terms of reliability and electrical conductivity<sup>1</sup>. While down-scaling transistors generally improves their performance, it actually increases the resistance and current density of the interconnects. This resulted in interconnects dominating the integrated circuit (IC) performance in terms of delay and power consumption<sup>2</sup>.

Carbon nanotubes (CNT) have been suggested as alternative for Cu and W metallization, especially for vertical interconnects (vias) as CNT can easily be grown vertical<sup>3</sup>. CNT have been shown to have excellent electrical reliability, allowing an up to 1,000 times higher current density than Cu<sup>4</sup>. Moreover, CNT do not suffer from surface and grain boundary scattering, which is increasing the resistivity of Cu at the nanometer scale<sup>5</sup>. Finally, CNT have been shown to be excellent thermal conductors<sup>6</sup>, which can aid in the thermal management in VLSI chips.

For successful integration of CNT in VLSI technology it is important that the growth processes for the CNT is made compatible with semiconductor fabrication. This requires the low temperature growth of CNT (< 400 °C) using materials and equipment which are considered compatible and scalable to large scale manufacturing. While many examples of CNT test vias have been demonstrated in the literature<sup>7,8,9,10,11,12,13,14</sup>, most of these use Fe as catalyst which is regarded as a contaminant in IC manufacturing<sup>15</sup>. Besides, the growth temperature used in many of these works is much higher than the upper limit of 400 °C. Preferably CNT should even be grown below 350 °C, in order to allow integration with modern low-k dielectrics or flexible substrates.

Here we present a scalable method for growing CNT at temperatures as low as 350 °C using Co as catalyst<sup>16</sup>. This method is of interest for fabricating different electrical structures consisting of vertically aligned CNT in integrated circuits, ranging from interconnect and electrodes to super capacitors and field emission devices. The Co catalyst metal is often used in IC manufacturing for the fabrication of silicide's<sup>17</sup>, while TiN is an often used barrier material<sup>7</sup>. Moreover, we demonstrate a process for fabricating CNT test vias while only using techniques from standard semiconductor manufacturing. With this, CNT test vias are fabricated, inspected by scanning electron microscopy (SEM) and Raman spectroscopy, and electrically characterized.

## Protocol

Caution: Please consult all relevant material safety data sheets (MSDS) before use. Several of the chemicals used in this fabrication process are acutely toxic and carcinogenic. Nanomaterials may have additional hazards compared to their bulk counterpart. Please use all appropriate

safety practices when working with equipment, chemicals or nanomaterials, including the use of engineering controls (fume hood) and personal protective equipment (safety glasses, gloves, cleanroom clothes).

## 1. Alignment Marker Definition for Lithography

1. Start with single-sided polished industrial grade Si(100) wafers with either n or p-type doping.
2. Coat the wafer with 1.4  $\mu\text{m}$  of positive photoresist. Perform a 90 sec hexamethyldisilazane (HMDS) treatment at 130 °C to promote adhesion of the photoresist, followed by cooling of the wafer on a cold plate, spin-coating at the appropriate speed (3,500 rpm), and a 90 sec soft bake at 95 °C.
3. Using a photo-lithography mask and exposure tool expose the alignment markers, exposure dose 120  $\text{mJ}/\text{cm}^2$ .
4. Perform a single puddle development process. Perform a 90 sec 115 °C post-exposure bake, followed by 60 sec development using developer and 90 sec hard bake at 100 °C to cure the resist.
5. Use a microscope to inspect if the openings in the resist are of the correct dimensions.
6. Etch 120 nm of Si using chlorine plasma etching. This thickness gives good contrast for the automatic alignment systems of the exposure tool used in this work. For example using an inductive coupled plasma (ICP): 20/40 sccm  $\text{O}_2/\text{CF}_4$ , 5 mTorr, 60/500 W platen/ICP RF power, 10 sec oxide breakthrough etching, followed by 80/40 sccm  $\text{Cl}_2/\text{HBr}$ , 60 mTorr, 20/500 W platen/ICP RF power, 35 sec Si etch.
7. Use an oxygen plasma stripper to remove the photoresist (1 kW, 400 sccm  $\text{O}_2$  with endpoint detection and 2 min overetch). As the photoresist is cured by the plasma normal solvent like acetone cannot be used.
8. Clean the wafers. First put them for 10 min in 99%  $\text{HNO}_3$ , followed by rinsing in DI water till the resistivity of the water is 5 M $\Omega$  (organic clean). After this clean the wafers for 10 min in 65%  $\text{HNO}_3$  at 110 °C, followed by rinsing with DI water till the resistivity of the water is 5 M $\Omega$  (metal clean). Use a rinser dryer to dry the wafers.

## 2. Bottom Metal and Interlayer Dielectric Deposition

1. Use magnetron sputtering to deposit the bottom metal layer of the test via. A stack of three metal layers needs to be deposited: 500 nm of Ti, 50 nm of TiN, and 100 nm Ti. The first Ti layer is to reduce the resistance of the stack, the TiN is the actual support layer for CNT growth, and the top Ti is to protect the TiN against plasma damage when etching the  $\text{SiO}_2$  layer<sup>12</sup>. Perform Ti sputtering using a pure Ti target with Ar-plasma at a substrate temperature of 350 °C. For TiN reactive sputtering use a combination of Ar and  $\text{N}_2$ , again at 350 °C substrate temperature.
2. Using plasma-enhanced chemical vapor deposition (PECVD), deposit a 1  $\mu\text{m}$  thick layer of  $\text{SiO}_2$ . Here tetraethyl orthosilicate (TEOS) is used as precursor at a platen temperature of 350 °C.
  1. Check the thickness of the  $\text{SiO}_2$  layer using an appropriate tool, for instance a reflectometer or ellipsometer.
3. Coat the wafer with 1.4  $\mu\text{m}$  of positive photoresist, starting with a 90 sec HMDS treatment at 130 °C, followed by cooling of the wafer on a cold plate, spin-coating at the appropriate speed (3,500 rpm), and a 90 sec soft bake at 95 °C.
4. Using a photo-lithography mask and exposure tool, expose the desired pattern of openings, which will be later etched into the  $\text{SiO}_2$  to form the vias, aligned to the alignment markers, exposure dose 140  $\text{mJ}/\text{cm}^2$ .
5. Perform a single puddle development process starting with a 90 sec 115 °C post-exposure bake, followed by 60 sec development using developer and 90 sec hard bake at 100 °C.
6. Use a microscope to inspect if the openings in the resist are of the correct dimensions and if the overlay to the alignment markers is correct.
7. Plasma etch the contact openings in the  $\text{SiO}_2$ . For example, use a triode plasma etcher with  $\text{C}_2\text{F}_6/\text{CHF}_3$  36/144 sccm at 180 mTorr and 300 W RF power. If necessary, perform etch rate tests on a test wafer in order to minimize over etching to 5%-10% in time.  
Note: Although the Ti is resistant to reactive etching in this fluorine chemistry, prolonged exposure to the plasma will result in physical etching of the Ti layer. If the TiN layer is exposed to the plasma this will have a negative influence on the growth of the CNT<sup>12</sup>. Do not use wet etching as this will result in too much widening of the openings, making the top metallization in part 4 problematic.
8. Remove the sacrificial Ti layer by wet etching in 0.55% HF for 60 sec. After etching rinse the wafers with DI water till the water resistivity is 5 M $\Omega$  and use a rinser dryer to dry the wafers.  
Note: Using a microscope it can be checked if the Ti layer is etched, the TiN layer will have a gold-brown color while the Ti is metallic grey.

## 3. Catalyst Deposition and CNT Growth

1. Evaporate 5 nm of Co using an e-beam evaporator. Pump down till at least  $2 \times 10^{-6}$  Torr, and heat the wafers to 60 °C using lamps under vacuum before depositing to remove any water film. The photo-resist used to define the contact openings is kept on the wafer to provide self-alignment of the catalyst to the contact openings in the  $\text{SiO}_2$ .
2. Remove the Co outside the contact openings by lift-off. For Co it was found that tetrahydrofuran (THF) gives the best lift-off results and growth at low temperatures. *N*-methyl-2-pyrrolidone (NMP), which was previously used for lift-off after Fe evaporation, was found to damage the Co too such an extent to prevent any aligned CNT growth. Put the wafer for 15 min in an ultrasonic bath with THF at 35 °C. Rinse with DI water for 5 min and dry using a spinner or nitrogen gun.
3. Inspect the wafer underneath a microscope and check for resist residues. If residues remain perform a longer ultrasonic treatment in THF, and optionally use a special soft cotton swab for lift-off purposes to manually wipe away residues.
4. Perform CNT growth using low-pressure chemical vapor deposition (LPCVD). Use the following recipe: 8 min pre-anneal at 350 °C with 700 sccm  $\text{H}_2$  at 80 mbar, followed by CNT growth by adding 50 sccm  $\text{C}_2\text{H}_2$ . At 350 °C, 60 min of growth gives roughly 1  $\mu\text{m}$  of CNT. If necessary perform a test growth to tune the height, which should be the same thickness as the  $\text{SiO}_2$  layer. Cool down the reactor and purge using  $\text{N}_2$ .
5. Use a scanning electron microscope to check the height of the CNT inside the openings under 45° tilt, or by preparing a cross-section.
6. Inspect the samples using Raman spectroscopy to determine the crystallinity of the CNT<sup>18</sup>.

## 4. Topside Metallization

1. Use magnetron sputtering to deposit the top metal. As Ti is a good metal for contacting CNT<sup>19</sup>, first sputter 100 nm of Ti, followed by 2  $\mu\text{m}$  of Al (1% Si) without breaking the vacuum.
2. Coat the wafer with 3.1  $\mu\text{m}$  of positive photoresist with higher viscosity, starting with a 90 sec HMDS treatment at 130 °C, followed by cooling of the wafer on a cold plate, spin-coating at 3,000 rpm, and a 90 sec soft bake at 95 °C.
3. Using a photo-lithography mask and exposure tool expose the top metal pattern aligned to the alignment markers, exposure dose 420 mJ/cm<sup>2</sup>, focus of -1.
4. Perform a single puddle development process. This starts with a 90 sec 115 °C post-exposure bake, followed by 60 sec development using developer and 90 sec hard bake at 100 °C.
5. Use a microscope to inspect if the lines in the resist are of the correct dimensions and if the overlay to the markers is correct.
6. Etch the Ti/Al stack using chlorine plasma etching. For example using an inductive coupled plasma: 30/40 sccm Cl<sub>2</sub>/HBr, 5 mTorr, 40/500 W Platen/ICP RF power with endpoint detection and 80% overetch using 15/30 sccm Cl<sub>2</sub>/HBr.
7. Use an oxygen plasma stripper to remove the photoresist (1 kW, 400 sccm O<sub>2</sub> with endpoint detection and 2 min overetch). If the metal coverage is not complete (*i.e.*, there are pinholes around the CNT) use an organic solvent (*e.g.*, NMP) to remove the photoresist in order to prevent plasma damage to the CNT.
8. Clean the wafers. Put them for 10 min in 99% HNO<sub>3</sub>, followed by rinsing with DI water till the resistivity of the water is 5 M $\Omega$  (organic clean). Use a rinser dryer to dry the wafers.

## 5. Measurements

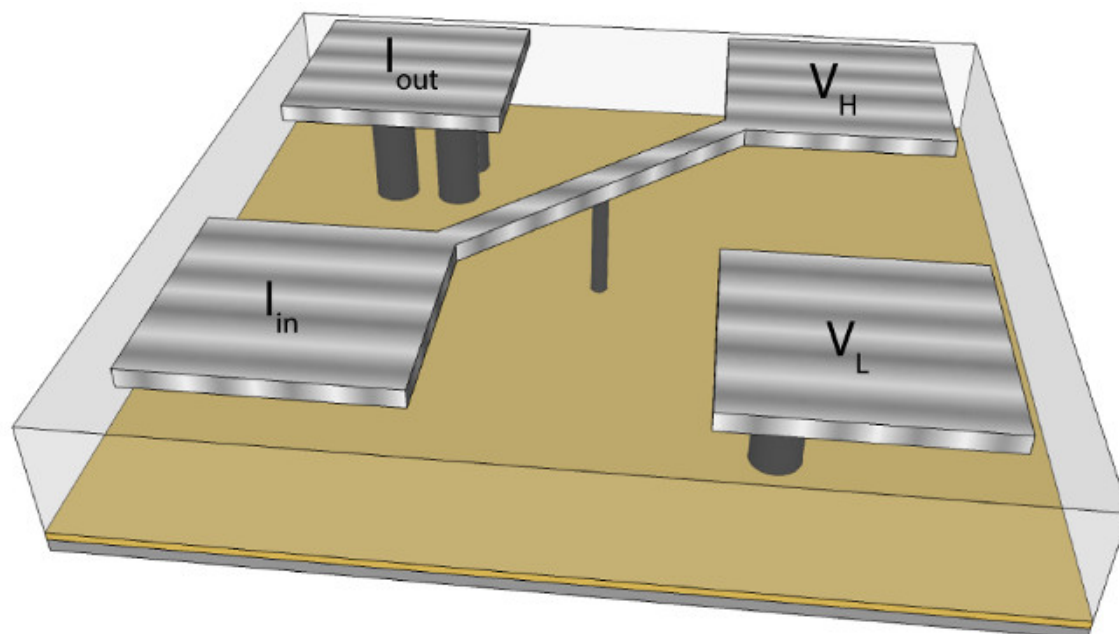
1. Use a scanning electron microscope according to manufacturer's instructions to check the top metallization of the wafers.  
Note: If necessary the wafer can be mechanically cleaved in order to check the complete CNT via using a sample tilt of 90°, resulting in images as shown in **Figure 3**. As the samples are electrically conductive no additional treatment steps have to be used and the samples can be directly mounted into the SEM. Generally, high acceleration voltages of 15 or 20 kV can be used, but if the SiO<sub>2</sub> layer is charging up too much this can be reduced to 5 kV.
2. Perform 4-point probe I-V measurements using a probe station in combination with a semiconductor parameter analyzer as described in **Figure 1** and in Vollebregt *et al.*<sup>16</sup>.  
Note: Normally a voltage sweep from -0.5 to 0.5 V is sufficient, as the potential drop over an interconnect ideally is small. By using a 4-point probe setup the contact resistance of the probe needles and the wire resistances of the setup are omitted.

## Representative Results

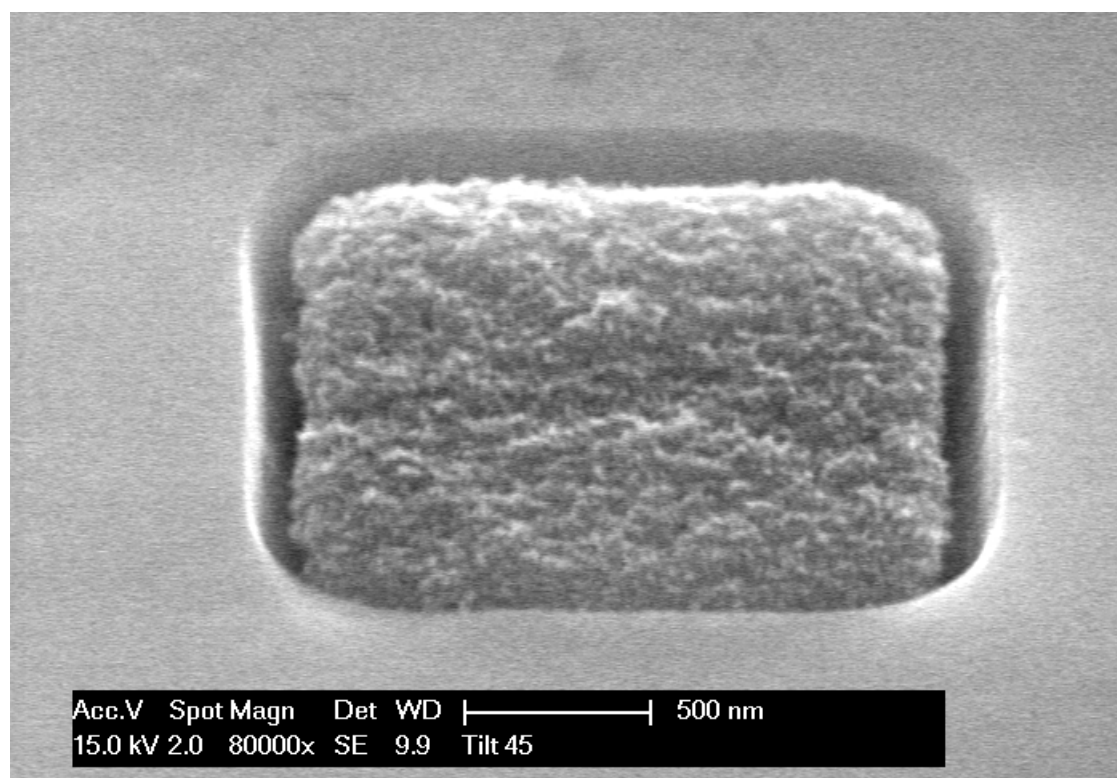
The design of the measurement structure used in this work can be found in **Figure 1**. By employing such a structure the measurement of the CNT bundle resistance and the metal-CNT contact resistances can be determined accurately, as probe and wire resistances are circumvented. The resistance of the bundle is a measure for the quality and density of the CNT bundle. In order to determine the contact resistance bundles of different lengths should be measured.

A typical SEM image of CNT grown at 350 °C for 60 min taken from the top before metallization at 45° tilt is shown in **Figure 2**. Such an image is useful for checking if the growth time of the CNT is correctly set in order to obtain the same length as the thickness of the SiO<sub>2</sub> layer. A cross-section prepared by mechanical cleaving inspected by SEM of the same wafer after metallization is shown in **Figure 3**. This can be used to determine the alignment of the CNT, their density (for instance by counting the number of CNT per unit length), and if a high resolution SEM is used to determine their diameter. Also the contact area between the CNT and the metal layers can be investigated.

Raman spectra of Co-grown CNT at 350 °C is displayed in **Figure 4**. Raman spectroscopy is a powerful technique for investigating the crystallinity of the CNT<sup>18</sup>, and can for instance be used to optimize the CNT growth parameters in order to obtain the highest quality CNT. I-V measurements were performed using four point probe structures and are displayed in **Figure 5**. When the I-V behavior is linear it indicates ohmic contact between the CNT and the metal contacts. From the slope the electric resistance can be determined. From the resistance and the dimension of the bundles the resistivity can be calculated, which for these CNT bundles is compared to the literature in **Figure 6**.

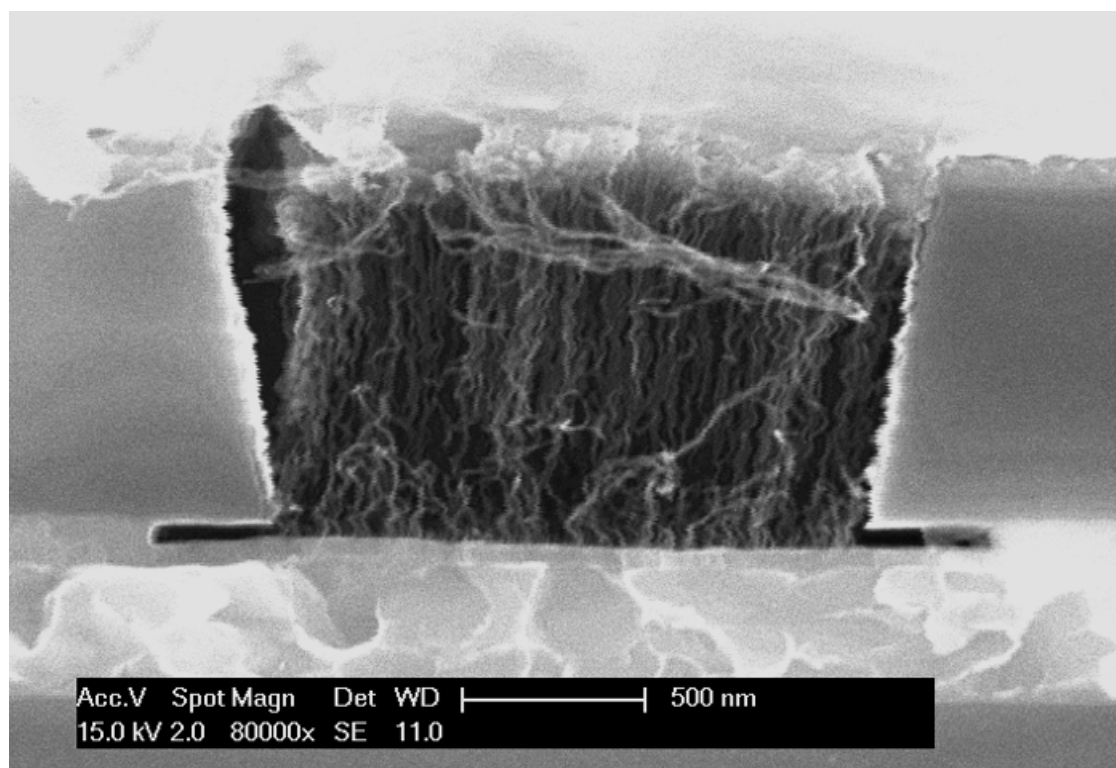


**Figure 1. Design of 4-point probe measurement structure used in this work.** In the figure the dark yellow layer indicates the TiN, the black tubes the CNT bundles, and the metallic layer the Ti and Al stack. The sacrificial Ti layer is omitted for clarity and the oxide is semi-transparent. Probe connections for electrical 4-point probe measurements are indicated. [Please click here to view a larger version of this figure.](#)

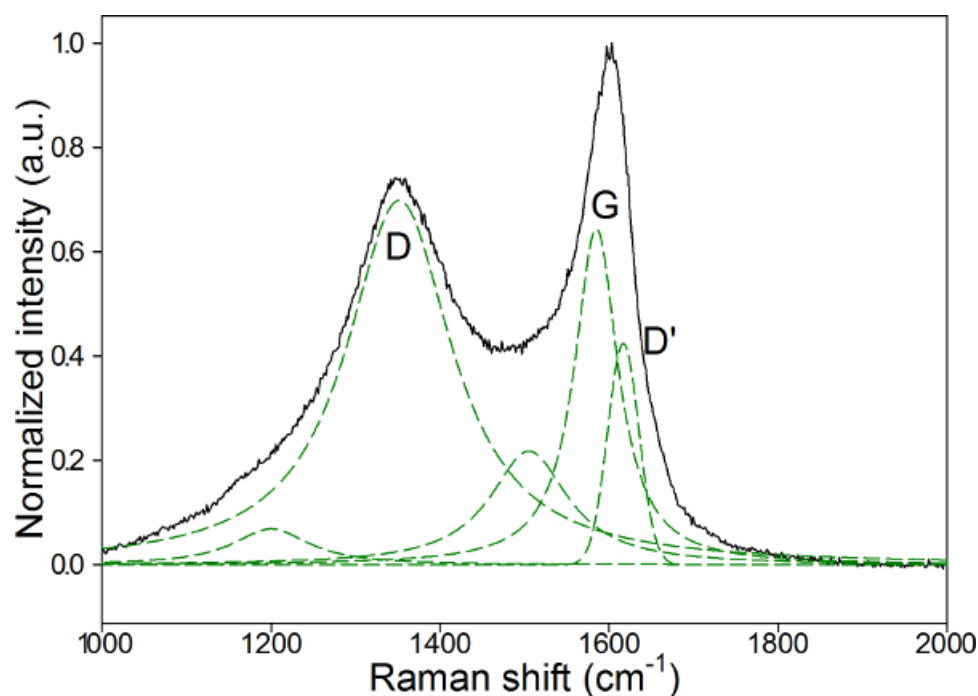


**Figure 2. Top-view SEM image of a CNT bundle.** This shows a 2  $\mu\text{m}$  wide CNT bundle grown in a contact opening which was etched inside the  $\text{SiO}_2$ . This figure has been modified from <sup>16</sup>, with permission from Elsevier. [Please click here to view a larger version of this figure.](#)

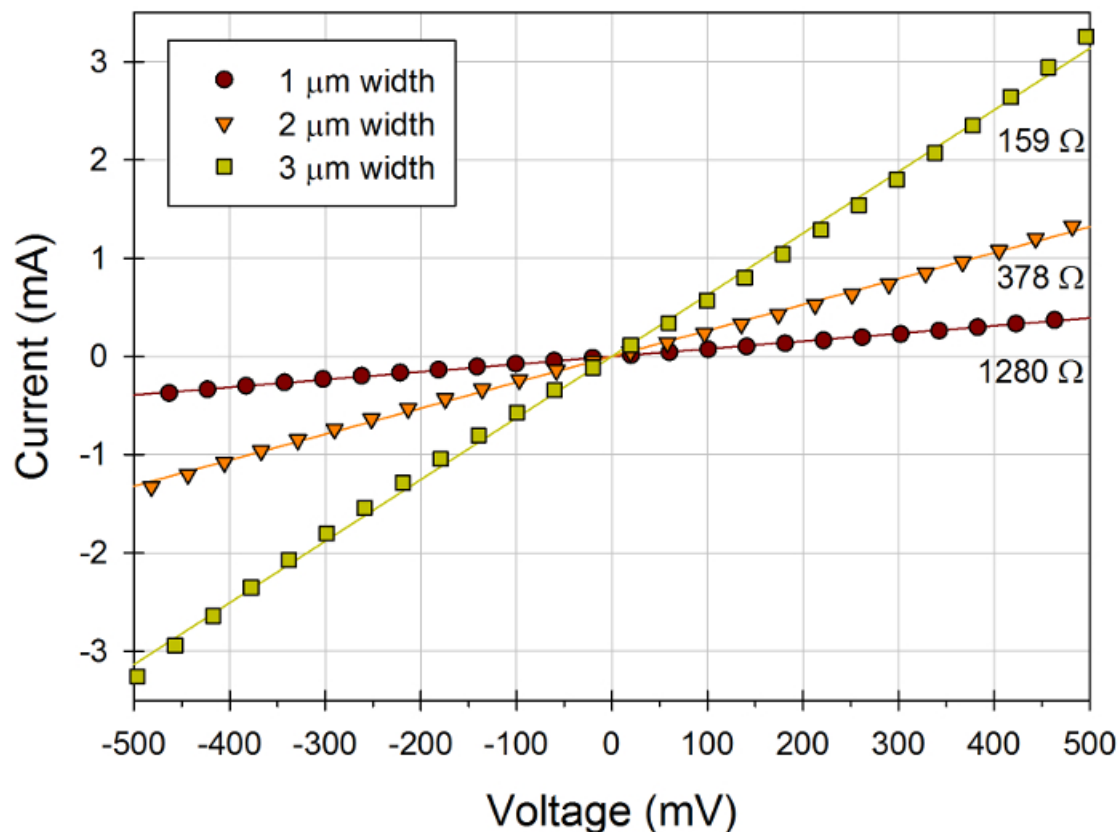




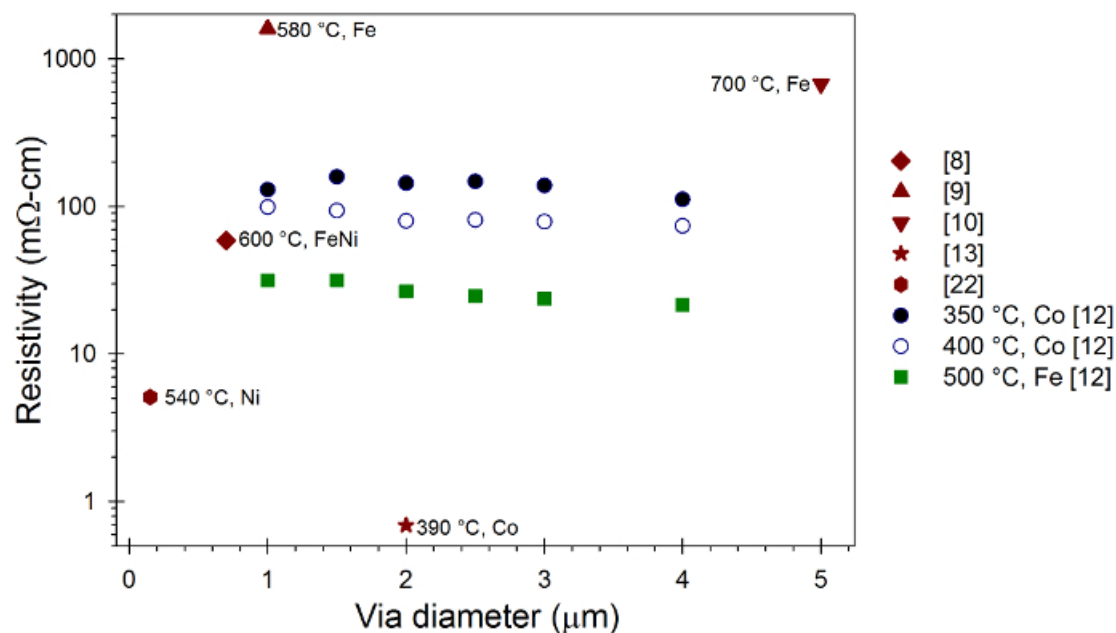
**Figure 3. SEM cross-section of CNT test via.** Cross-section of a 2  $\mu\text{m}$  wide and 1  $\mu\text{m}$  long CNT test via prepared using mechanical cleaving after metallization. This figure has been modified from <sup>16</sup>, with permission from Elsevier. [Please click here to view a larger version of this figure.](#)



**Figure 4. Raman spectrum of a CNT bundle grown using Co at 350 °C.** The names of the Raman bands are indicated. The black curve displays the raw measurement data. For all bands a Lorentzian fitting is performed (green dashed curves), except for the D' band which is fitted by a Gaussian<sup>18</sup>. [Please click here to view a larger version of this figure.](#)



**Figure 5. I-V measurements of CNT test vias with different diameters.** The symbols represent the measurement data, while the solid line indicates a linear least squares fitting to the measurement data. The electrical resistances of the different vias as determined from the slope of the linear fitting are indicated. This figure has been modified from <sup>16</sup>, with permission from Elsevier. [Please click here to view a larger version of this figure.](#)



**Figure 6. Comparison of CNT bundle resistivity with values from the literature.** The resistivity is calculated from the resistance and the via dimensions. It is compared with values from the literature, and CNT vias fabricated at different temperatures using the method described in this work. This figure has been modified from <sup>16</sup>, with permission from Elsevier. [Please click here to view a larger version of this figure.](#)

## Discussion

**Figure 1** displays a schematic overview of the structure fabricated in this work, and which was used for the 4-point probe measurements. As the potential is measured through probes carrying no current, the exact potential drop ( $V_H - V_L$ ) over the central CNT bundle and its contacts to the metal can be measured. Bigger diameter CNT bundles are used to contact the bottom TiN layer from the contact pads, in order to reduce the total resistance for the current forcing probes and maximize the potential drop over the central CNT bundle.

As can be seen from **Figure 2**, the CNT were successfully grown inside the openings etched in the  $\text{SiO}_2$  with a length approximately the same as the depth of the hole (1  $\mu\text{m}$ ). It is crucial that the length of the CNT is roughly the same as the depth of the hole, in order to achieve conformal coating of the top metal contact. The bundles appear uniform, which also aids in conformal coating of the metal. The straightness and vertical alignment of the tubes can clearly be seen in the cross-section displayed in **Figure 3**. By counting, the density of the CNT bundle was estimated to be around  $5 \times 10^{10}$  tubes/ $\text{cm}^2$ . Using transmission electron microscopy the average diameter of the tubes was found to be 8 nm, as was shown elsewhere<sup>16</sup>. Due to the low growth temperatures the CNT walls contain many defects making determining the number of walls difficult. The tubes appear to have a hollow core, although bamboo crossings have been observed. The cross-section also shows the bottom TiN layer, and the sacrificial Ti layer which is partly removed underneath the  $\text{SiO}_2$  during the wet etching. If openings are placed closed together the etching time of the sacrificial Ti layer may have to be optimized to minimize underetch to prevent oxide delamination. Due to the dry etching of the hole, the spacing between the  $\text{SiO}_2$  and CNT bundle is minimal, which is essential to prevent the sputtered Ti and Al from forming short circuits around the CNT bundle.

Using the Raman data the crystallinity (or quality) of the CNT can be investigated. As the different Raman bands are close to each-other deconvolution of the bands is necessary, as described elsewhere<sup>18</sup>. From the Raman data in **Figure 4** it is apparent that a strong D and D' band can be observed, which are caused by Raman scattering with defects, while the G band is related to the C-C bond. The other two bands are weak Raman features which are included for more accurate fitting.

It is known that a low growth temperature in general results in a lower CNT quality<sup>18</sup>. Usually the D over G intensity ratio ( $I_{D/G}$ ) is used to assess the quality of graphitic materials, which is 1.1 in **Figure 4**. As has been shown by for instance Ferrari and Robertson<sup>20</sup>, care has to be taken when using only this band ratio. With increasing quality of the CNT, first the  $I_{D/G}$  ratio increases, till a certain amount of crystallization is reached after which the ratio decreases monotonically. Due to the very low growth temperature, the CNT in this work appear to have a crystallinity below this threshold<sup>16</sup>. In these cases the full-width at half maximum of the D band can be used to compare CNT samples fabricated at different process conditions<sup>18</sup>. It can be expected that the low quality of the CNT will significantly influence the electrical performance.

Judging from the almost complete linear behavior of the I-V characteristics in **Figure 5**, the contacts between the CNT and the top and bottom metal layers are ohmic. The resistance of the bundle decreases with diameter, which is to be expected as more CNT can conduct in parallel for larger bundles. The good contact between the CNT and the metals is attributed to the use of Ti<sup>19</sup>, and TiN which is more resilient against oxidation<sup>21</sup>. Besides, we found that due to the lack of any dielectric covering steps of the CNT after growth (using for instance spin-on glass), something which is often used in the literature in combination with chemical mechanical polishing (CMP)<sup>22,23</sup>, the contact resistance to the CNT is low due to embedding of the CNT tips in the top metal<sup>24</sup>.

When comparing the resistivities of the CNT bundles with literature, as is done in **Figure 6**, the results are among the average values in the literature. However, the growth temperature used in this work is record-low. The results of Yokoyama *et al.*<sup>13</sup> are the lowest resistivity reported in the literature, using only a 40 °C higher growth temperature. However, the equipment used for Co particle deposition in their work is likely not scalable to large volume manufacturing. Clearly the resistivity decreases with increasing growth temperature, which can be advantageous for application allowing higher growth temperatures. When comparing the resistivity of the CNT bundles with traditional interconnect metals like Cu (1.7  $\mu\Omega\text{-cm}$ ), it is apparent that a drastic reduction of the resistivity is required. Improving the quality of the CNT and the bundle density, by optimizing the growth conditions, will be required. This has to be done without increasing the growth temperature, in order to allow integration with modern low- $\kappa$  materials and flexible substrates.

We have thus demonstrated a technique for integrating low temperature CNT growth and integration into standard semiconductor fabrication. This technique has been used to fabricate CNT via test structures and has recently been applied for the fabrication of CNT super capacitors<sup>25</sup>.

## Disclosures

The authors have nothing to disclose.

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