Video Article

Fabrication of Gate-tunable Graphene Devices for Scanning Tunneling Microscopy Studies with Coulomb Impurities

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Abstract

Owing to its relativistic low-energy charge carriers, the interaction between graphene and various impurities leads to a wealth of new physics and degrees of freedom to control electronic devices. In particular, the behavior of graphene's charge carriers in response to potentials from charged Coulomb impurities is predicted to differ significantly from that of most materials. Scanning tunneling microscopy (STM) and scanning tunneling spectroscopy (STS) can provide detailed information on both the spatial and energy dependence of graphene's electronic structure in the presence of a charged impurity. The design of a hybrid impurity-graphene device, fabricated using controlled deposition of impurities onto a back-gated graphene surface, has enabled several novel methods for controllably tuning graphene's electronic properties.[1-8] Electrostatic gating enables control of the charge carrier density in graphene and the ability to reversibly tune the charge[2] and/or molecular[5] states of an impurity. This paper outlines the process of fabricating a gate-tunable graphene device decorated with individual Coulomb impurities for combined STM/STS studies.[2-5] These studies provide valuable insights into the underlying physics, as well as signposts for designing hybrid graphene devices.

Video Link

The video component of this article can be found at https://www.jove.com/video/52711/

Introduction

Graphene is a two-dimensional material with a unique linear band structure, which gives rise to its exceptional electrical, optical, and mechanical properties.[1,9-16] Its low-energy charge carriers are described as relativistic, massless Dirac fermions[15], whose behavior differs significantly from that of non-relativistic charge carriers in traditional systems.[15-18] Controlled deposition of a variety of impurities onto graphene provides a simple yet versatile platform for experimental studies of the response of these relativistic charge carriers to a range of perturbations. Investigations of such systems reveal that graphene impurities can shift the chemical potential[6,7], alter the effective dielectric constant[8], and potentially lead to electronically mediated superconductivity[9]. Many of these studies[6-8] employ electrostatic gating as a means to tuning the properties of the hybrid impurity-graphene device. Electrostatic gating can shift the electronic structure of a material with respect to its Fermi level without hysteresis.[2-5] Moreover, by tuning the charge[2] or molecular[5] states of such impurities, electrostatic gating can reversibly modify the properties of a hybrid impurity-graphene device.

Back-gating a graphene device provides an ideal system for investigation by scanning tunneling microscopy (STM). A scanning tunneling microscope consists of a sharp metal tip held a few angstroms away from a conductive surface. By applying a bias between the tip and the surface, electrons tunnel between the two. In the most common mode, constant current mode, one can map the topography of the sample surface by raster-scanning the tip back and forth. Additionally, the local electronic structure of the sample can be studied by examining a differential conductance *dI/dV* spectrum, which is proportional to local density of states (LDOS). This measurement is often termed scanning tunneling spectroscopy (STS). By separately controlling the bias and back-gate voltages, the response of graphene to impurities can be studied by analyzing the behavior of these *dI/dV* spectra.[2-5]

In this report, the fabrication of a back-gated graphene device decorated with Coulomb impurities (*e.g.,* charged Ca atoms) is outlined. The device consists of elements in the following order (from top to bottom): calcium adatoms and clusters, graphene, hexagonal boron nitride (h-BN),

silicon dioxide (SiO_2), and bulk silicon (**Figure 1**). h-BN is an insulating thin film, which provides an atomically flat and electrically homogeneous substrate for the graphene.[19-21] h-BN and SiO_2 act as dielectrics, and bulk Si serves as the back-gate.

To fabricate the device, graphene is first grown on an electrochemically polished Cu foil[22,23], which acts as a clean catalytic surface for the chemical vapor deposition (CVD)[22-25] of graphene. In a CVD growth, methane (CH_4) and hydrogen (H_2) precursor gases undergo pyrolysis to form domains of graphene crystals on the Cu foil. These domains grow and eventually merge together, forming a polycrystalline graphene sheet.[25] The resulting graphene is transferred onto the target substrate, an h-BN/SiO_2 chip (prepared by mechanical exfoliation[19-21] of h-BN onto an SiO_2/Si(100) chip), *via* poly(methyl methacrylate) (PMMA) transfer.[26-28] In the PMMA transfer, the graphene on Cu is first spin-coated with a layer of PMMA. The PMMA/graphene/Cu sample then floats on an etchant solution (*e.g.,* $FeCl_3$ (aq)[28]), which etches away the Cu. The unreacted PMMA/graphene sample is fished with an h-BN/SiO_2 chip and subsequently cleaned in an organic solvent (*e.g.,* CH_2Cl_2) and Ar/H_2 environment[29,30] to remove the PMMA layer. The resulting graphene/h-BN/SiO_2/Si sample is then wire-bonded to electrical contacts on an ultra-high-vacuum (UHV) sample plate and annealed in an UHV chamber. Finally, the graphene device is deposited *in situ* with Coulomb impurities (*e.g.,* charged Ca atoms) and studied by STM.[2-5]

Protocol

1. Electrochemical Polishing of a Cu Foil[22,23]

Note: Electrochemical polishing exposes bare Cu surface for graphene growth by removing the protective surface coating and controls the growth seed density.

1. Prepare an electrochemical polishing solution by mixing 100 ml ultra-pure water, 50 ml ethanol, 50 ml phosphoric acid, 10 ml isopropanol, and 1 g urea.
2. Cut Cu foil into multiple 3 cm by 3 cm foils. Note: Each foil serves as either an anode or a cathode.
3. Set up the anode/cathode by clipping a Cu foil vertically with a holder and connecting it to the appropriate terminal of the power supply. Note: The anode (positive terminal) will be electrochemically polished for graphene growth.
4. Before the polishing begins, set constant voltage of 4.8 V in the power supply.
5. Turn on the power supply as soon as the anode and the cathode are simultaneously dipped into the electrochemical polishing solution. Separate the electrodes by about 2 cm. Check that the resulting current is between 1-2 A.
6. Stop electrochemical polishing after 2 min by turning off the power supply. Take out the anode and immediately rinse it separately with ultra-pure water, acetone, and isopropanol.
7. Blow-dry the rinsed Cu foil with N_2 gas and store it in a dry container.

2. Chemical Vapor Deposition (CVD) of Graphene on a Cu Foil[22-25]

1. Place a quartz tube in a CVD furnace and connect the tube to the rest of the gas line with KF fittings.
2. Place an electrochemically polished Cu foil on top of a quartz boat. Using a long rod, push the quartz boat into the quartz tube until the Cu foil is placed at the center of the CVD furnace. Enclose the system with KF fittings.
3. Pump down the system with a roughing pump. Purge the system with H_2.
4. Ramp up the temperature to 1,050 °C with 200 sccm of H_2. Anneal at 1,050 °C with the same gas flow for 2 hr. Note: The temperature is measured via built-in Type K thermocouple in a tube furnace.
5. Cool down to 1,030 °C with the same gas flow. Grow graphene for 10 min with 40 sccm CH_4 and 10 sccm H_2.
6. As soon as the growth is over, open up the furnace hood to cool rapidly down toRT. Keep the same gas flow.
7. Once the temperature is below 100 °C, turn off the gas flow.
8. Turn off the pump. Vent the system with N_2 gas by slowly opening the metering valve between the gas line and the N_2 gas cylinder.
9. Take out the sample. Cut the Cu foil into pieces with desired dimensions.
10. Store the sample in a dry container inside a desiccator.

3. Mechanical Exfoliation[19-21] of h-BN onto a SiO_2 Chip

1. Clean an SiO_2 chip. Note: The SiO_2 chip consists of a roughly 285 nm thick SiO_2 layer on top of a bulk Si.
    1. Cut a SiO_2 wafer into about 1 cm by 1 cm chips using a diamond scribe.
    2. Rinse the SiO_2 chip with water and isopropanol. Keep the SiO_2 surface covered with water/isopropanol after each rinse.
    3. Place the SiO_2 chip on the spin coater to remove liquid from its surface. Spin the chip with 3,000 rpm for 15 sec.
    4. Check the cleanliness of the chip under an optical microscope with dark field setting. Note: Under dark field setting, solid impurities appear as bright particles.
2. Place a clean SiO_2 chip, exfoliation tape, and h-BN crystal on a clean table with an optical microscope.
3. Prepare two strips of tape: a parent tape and a second tape. Place both on the table with their sticky sides up. Place a h-BN crystal on the sticky side of the parent tape.
4. Place the sticky side of the second tape over the h-BN crystal on the parent tape (so that sticky sides of the second and parent tapes are touching). Rub over the crystal gently to remove trapped air bubbles.
5. Peel the second tape off to exfoliate the h-BN crystal onto the second tape. Store the parent tape for future use.
6. Fold the second tape onto itself, rub gently over the crystal, and peel off the tape. Repeat this process 10 times, folding the second tape so that the h-BN crystals are transferred to a fresh new region of the second tape each time.
7. Place a clean SiO_2 chip under the microscope. Stick the region of the second tape containing the h-BN crystal onto the SiO_2 chip. Ensure that the tape also sticks to the microscope stand for securing the chip during the upcoming exfoliation step.

8. Slowly peel off the tape, monitoring the process under the microscope. As the tape is nearly peeled off, use a tweezer to hold the SiO_2 chip in place. Note: Peeling too fast will result in less h-BN flakes on the chip.
9. Once the tape is peeled off, place the chip inside a CVD furnace. Anneal the chip in air at 500 °C for 2 hr.

4. Poly(methyl methacrylate) (PMMA)[26-28] Transfer of Graphene onto h-BN/SiO_2

1. Put one drop of PMMA (A4) on the graphene/Cu/graphene foil. Spin-coat the foil with 3,000 rpm in 30 sec. Note: As $FeCl_3$ (aq) etches away the Cu layer during the upcoming etching step, the backside graphene will fall off while the PMMA/graphene layer will remain unreacted (**Figure 2**).
2. Using a $FeCl_3$ resistant spoon, let the spin-coated Cu foil float on the following solutions in this order: 1.5 min on $FeCl_3$ (aq), 5 min on ultra-pure water, 1 min on $FeCl_3$ (aq), 5 min on ultra-pure water, 15 min on $FeCl_3$ (aq), 5 min on ultra-pure water, 5 min on ultra-pure water, and 30 min on ultra-pure water. Prepare each ultra-pure water bath in a separate beaker.
3. Fish the PMMA/graphene sample with a h-BN/SiO_2 chip. Place it on a hot plate at 80 °C for 10 min to remove water and at 180 °C for 15 min to relax[27] PMMA film.
4. Place the PMMA/graphene/h-BN/SiO_2 chip in CH_2Cl_2 O/N to dissolve the PMMA layer.

5. Ar/H_2 Annealing[29,30]

1. Place the quartz tube on the CVD furnace and connect the tube to the rest of the gas line with KF fittings.
2. Place the graphene/BN/SiO_2 chip on a quartz boat. Using a long rod, push the quartz boat into the quartz tube until the chip is placed at the center of the CVD furnace. Enclose the system with KF fittings.
3. Pump down the system with a roughing pump. Purge the system with H_2 and Ar.
4. Build up the pressure to 1 atm with 100 sccm H_2 and 200 sccm Ar with a metering valve. Once the pressure reaches 1 atm, adjust the aperture size of the metering valve to stabilize the pressure at 1 atm.
5. Ramp up the temperature to 350 °C and anneal for 5 hr with the same gas flow.
6. Cool down to RT with the same gas flow.
7. Once the temperature is below 100 °C, turn off the gas flow. Close all valves.
8. Turn off the pump. Vent the system with N_2 gas by slowly opening the metering valve between the gas line and the N_2 gas cylinder.
9. Take out the sample. Check the number of graphene layers and defect level with Raman spectroscopy[32]. Check its cleanliness/uniformity under optical microscope. Scan multiple areas that appear clean under the optical microscope with atomic force microscope (AFM) to ensure that the sample appears clean/uniform at a small length scale (<500 nm) as well.
10. Store it in a dry container inside a desiccator.

6. Assembling a Gate-tunable Graphene Device for STM Measurement[2-5]

1. Evaporate a 50 μm by 50 μm Au/Ti contact pad onto the Ar/H_2-annealed CVD graphene/h-BN/SiO_2 sample.
    1. Tape the sample onto a stage on top of a micromanipulator.
    2. While monitoring with optical microscope, align a stencil mask with graphene using the micromanipulator so that the Au/Ti contact will be deposited near the region of interest without covering the surface.
    3. Transfer the sample with stencil mask to an e-beam evaporator. Evaporate 10 nm of Ti at 3 Å/sec. Cover up the Ti layer by evaporating 30-50 nm of Au at 3 Å/sec in the same evaporation session without breaking vacuum. Note: Alternatively, 1 nm of Cr is a good substitute for the 10 nm of Ti.
    4. Transfer the sample with stencil mask back to the micromanipulator for removing the stage.

2. Mount the sample onto an ultra-high-vacuum (UHV) sample plate.
    1. Place a thin piece of sapphire on a UHV sample plate. Note: The sapphire acts as an insulating layer that prevents electrical contact between the Si and STM ground. Furthermore, sapphire is an excellent thermal conductor for the purpose of sample annealing.
    2. Place the sample on top of the sapphire. Place another thin piece of sapphire on the sample. Make sure that the sapphire does not cover the graphene surface.
    3. Secure the sapphire/sample/sapphire structure with a metallic clamp. Ensure that the entire structure is rigid or else it will vibrate inside a STM.

3. Wire-bond the UHV sample plate terminals to appropriate contacts on the graphene device. Note: The deposited Au/Ti electrodes are wire-bonded to ground while the Si bulk is wire-bonded to the gate electrode (**Figure 1**).
    1. Place the mounted sample on a grounded wire-bonding stage.
    2. Identify locations of the Au/Ti contacts using an optical microscope.
    3. Turn on a wire-bonder. If the wire-bonder is pneumatic, turn on N_2 gas. Set the wire-bonder to make two bonds.
    4. Using a wire-bonding arm, place the tip of the wire bonder on top of the appropriate terminal on the UHV sample plate. Move down and gently press the tip of the wire bonder onto the terminal until the wire-bonder indicates that the bonding is finished.
    5. Thread a wire to the Au/Ti contact on the graphene device. Move down and gently press the tip of the wire bonder onto the Au/Ti contact until the wire-bonder indicates that the bonding is finished.
    6. Use a diamond scribe to scratch off some SiO_2 on the edge of the SiO_2 chip to expose the Si that will be used as a back-gate. Repeat the two-bonding process for the exposed Si.
    7. Insert the sample inside a UHV (10^{-10} Torr) prep chamber and anneal the wire-bonded graphene device at around 300 °C. Transfer the device to a STM chamber.

Note: The graphene device should be annealed until its surface appears clean under STM (see Sec. 8 of the Protocol). The annealing time will vary depending on the initial cleanliness of the device.

7. STM Tip Calibration on Au(111) Surface[31]

1. Anneal/sputter an Au(111) sample on the heater stage in a UHV chamber to clean/flatten the Au surface. Anneal for 5 min at 375 °C, and sputter for 5 min with Ar^+ beam accelerated to 500 V. Transfer the Au(111) sample to the STM scanning stage.
2. Approach an Au(111) surface with a STM tip. Apply 10 V pulses on the STM tip until an Au(111) herringbone reconstruction is clearly visible.
3. Calibrate the tip by adjusting the tip shape and comparing the differential conductance *dI/dV* spectrum to the standard Au(111) *dI/dV* spectrum.[31]
    1. Scan the Au(111) surface with 40 nm by 40 nm frame to identify a clean/flat area. If the surface has a high density of step edges, move to a new area for scanning.
    2. Gently crash the STM tip 0.4 to 1.0 nm into a clean region of the Au(111) surface; this controlled crashing is referred to as a “poke.” Turn off the feedback and click “Take Spectroscopy” button to take a *dI/dV* spectrum *via* lock-in onto the current response of an ac modulated voltage (6 mV and 613.7 Hz) added to the tip bias.
    Note: Once ac modulated voltage (6 mV and 613.7 Hz) is provided on the tip, the resulting tunneling current goes into the lock-in amplifier, which isolates the component of the current with the same frequency and returns *dI/dV* signal. By recording this signal as the sample bias is swept from -1.0 to 1.0 V, *dI/dV* spectrum is generated. Because this spectroscopy program is home-written, the instruction for taking the spectroscopy will vary among different programs.
    3. Check the obtained *dI/dV* curve against a standard Au(111) *dI/dV* spectrum (**Figure 4**). Make sure the Au(111) surface state is present in the *dI/dV* curve and that the spectrum is absent of any anomalous feature. If the measured *dI/dV* curve is not acceptable, repeat the poke in step 7.3.2 until the *dI/dV* curve looks like the one shown in **Figure 4**.
    4. Once tip shape and *dI/dV* spectrum are optimized, wait 15 to 30 min; if the STM tip is unstable, *dI/dV* spectrum will change during this time interval. Retake a *dI/dV* spectrum at a different location to confirm whether the STM tip is stable or not.
    5. Repeat the poke in step 7.3.2 if *dI/dV* curve has changed. Proceed to scan graphene if *dI/dV* curve is unchanged.

8. Scanning Graphene

1. Transfer the graphene device to a STM scanning stage.
2. Use a long-distance optical microscope to see the STM tip and graphene device. After laterally aligning the tip and h-BN flake of interest, approach the graphene.
3. Start scanning a 2 nm by 2 nm area. Slowly enlarge the scan window to 5 nm by 5 nm, 10 nm, by 10 nm, 15 nm by 15 nm, 20 nm by 20 nm, *etc.* If a large impurity (>100 pm in height) is encountered, withdraw the tip and move to a different area.
4. Take a *dI/dV* spectrum and compare to the standard *dI/dV* spectrum on graphene/h-BN substrate (see Ref. 21). If the spectrum is not comparable, recalibrate the tip on an Au(111) surface (see Sec. 7 of the Protocol).
5. Scan multiple areas to get a sense of how frequently large impurity (>100 pm in height) is encountered. Based on these statistics, deduce the cleanliness of the sample.

9. Depositing Coulomb Impurities on a Graphene Surface[2-4]

1. Obtain a Ca source. Calibrate the evaporation of Ca atoms with a residual gas analyzer (RGA) and quartz crystal microbalance (QCM) in an UHV test chamber. Note: RGA evaluates the purity of Ca deposit while QCM measures a Ca deposition rate.
    1. Run current through the Ca source.
    2. Increase the current until a Ca partial pressure of 10^{-10} Torr is detected in the RGA mass spectrum. Be aware of the fact that Ca and Ar have the same mass and therefore are indistinguishable in the RGA.
    3. Measure the Ca deposition rate (layer/sec) with the QCM.
        1. Input the density (*e.g.,* 1.55 g/cm^3 for Ca ion) of the deposit to convert frequency shift value to deposition rate.
        2. The deposition rate monitor for the QCM reads the deposition rate in /s; convert this to layer/sec by assuming that the thickness of a monolayer is equal to the ionic diameter (*e.g.,* 0.228 Å for Ca ion) of the deposit.
    4. Determine the optimal current by adjusting the current until the deposition rate monitor indicates a desired deposition rate (*e.g.,* 3.33 x 10^{-5} layer/sec).
2. Given the deposition rate (*e.g.,* 3.33 x 10^{-5} layer/sec) in step 9.1.3, calculate the time (sec) for depositing the desired amount (*e.g.,* 0.01 monolayer) of Ca. In the STM, deposit Ca on a Cu(100) surface *in situ* with the optimal current setting from step 9.1.3. Check the Ca coverage and cleanliness of the post-deposition Cu(100) surface with STM (see step 8.5); recalibrate the current setting until the Cu(100) surface condition under STM appears as expected.
Note: Deposition parameters are optimized on Cu(100) first to minimize the risk of contaminating the graphene device with poorly controlled deposition.
3. Transfer the graphene device to a STM for *in situ* deposition at 4 K.
4. Deposit charged Ca atoms onto the graphene surface.
    1. Before depositing Ca on graphene, outgass the Ca source. Slowly increase the current on the source by 0.25 A every 5-10 min until the desired current in step 9.2 is reached. Close a shutter between the graphene and Ca source to prevent outgassed contaminants from reaching the graphene.
    2. Let the evaporation flux stabilize for 20 min before opening the shutter.

3. Open the shutter and deposit desirable (*e.g.,* 0.01 monolayer) amount of Ca ions onto the graphene surface. Ensure that the graphene device has line-of-sight with the Ca source. Ensure that the STM tip is out of line-of-sight of the Ca source to prevent Ca atoms from sticking to the STM tip.

5. Check the Ca coverage and cleanliness of the post-deposition graphene surface with STM (see Step 8.5). Refer to Ref. 2, 3, and 4 for further protocol of the study of Coulomb impurities on graphene.

Representative Results

Figure 1 illustrates a schematic of a back-gated graphene device. Wire-bonding Au/Ti contact to an UHV sample plate grounds graphene electrically, while wire-bonding Si bulk to an electrode that connects to an external circuit back-gates the device. By back-gating a device, a charge state of a Coulomb impurity at a given sample bias (which is controlled by the STM tip) can be tuned to a different charge state.[2-4]

Figure 2 outlines the steps for fabricating a gate-tunable graphene device. A Cu foil is first electrochemically polished to remove its protective surface coating and modify its growth seed density.[23,24] After electrochemical polishing, the Cu foil should appear shinier under the naked eye than before as its surface should have become smoother. The electrochemically polished Cu foil then acts as a catalytic substrate for CVD growth of graphene. Graphene is then transferred onto an h-BN/SiO_2 substrate *via* PMMA transfer. The resulting sample is cleaned in an Ar/H_2 atmosphere and characterized (**Figure 3**). Subsequently, it is assembled into a back-gated device.

Before the sample is assembled into a back-gated device, the graphene surface is characterized by an optical microscope (**Figure 3A**), Raman spectroscopy (**Figure 3B**), and AFM (**Figure 3C**). With an optical microscope image, it is easy to examine the cleanliness, continuity, and the number of graphene layers throughout the entire sample. With a Raman spectrum, the number of graphene layers and defect level can be evaluated by examining the I_G:I_{2D} peak intensity ratio and D peak intensity, respectively.[32] With an AFM image, various features — cleanliness, uniformity, surface roughness, *etc*. — of the sample can be reliably evaluated at a small length scale (<500 nm). A good sample should appear clean, continuous, uniform, and monolayered under both optical microscope and AFM images. Moreover, a good sample should exhibit a minimal D peak intensity (a sign of minimal defect) and less than 1:2 ratio of I_G:I_{2D} peak intensity ratio (a sign of monolayer) under Raman spectroscopy.[32]

Before the device can be characterized under a STM, a STM tip must be calibrated on an Au(111) surface to decouple the STM tip states from the sample's surface states as much as possible. Without the tip calibration, the differential conductance *dI/dV* spectrum will appear convoluted due to a strong coupling between the tip states and the sample's surface states: in other words, STM data taken from an uncalibrated tip may not represent the real property of the sample. To calibrate the tip, the STM tip is repetitively pulsed/poked into an Au(111) surface until a high resolution image of herringbone reconstruction (**Figure 4A**) can be obtained and a *dI/dV* spectrum appears comparable to the standard Au(111) *dI/dV* spectrum (**Figure 4B**). The *dI/dV* spectrum should exhibit a sharp step at $V_{sample} \approx$ -0.5 V, which represents the onset of the Au(111) surface state. Moreover, the *dI/dV* spectrum should exhibit no anomalous peaks and dips, which may appear as artifacts when performing *dI/dV* measurements on graphene.

After the tip calibration, the sample surface is examined with STM. **Figure 5A** shows a Moiré pattern for graphene/h-BN, which arises from a mismatch in the lattice constants of graphene and h-BN. The wavelength of a Moiré pattern depends on the angle of rotation between the graphene and underlying h-BN lattices: smaller the twist angle, greater the wavelength. Appearance of Moiré pattern confirms the presence of clean graphene on an h-BN substrate. Once the sample surface is examined, Ca ions are deposited onto graphene, whose topography is shown in **Figure 5B**. A Moiré pattern appears in the background of the image. Once charged Ca atoms are successfully deposited, STM tip can construct artificial nuclei consisting of multiple charged Ca dimers by pushing each dimer into small clusters. STM study results for charged Co and Ca adatoms are shown in Ref. 2 & 3 and Ref. 4, respectively.

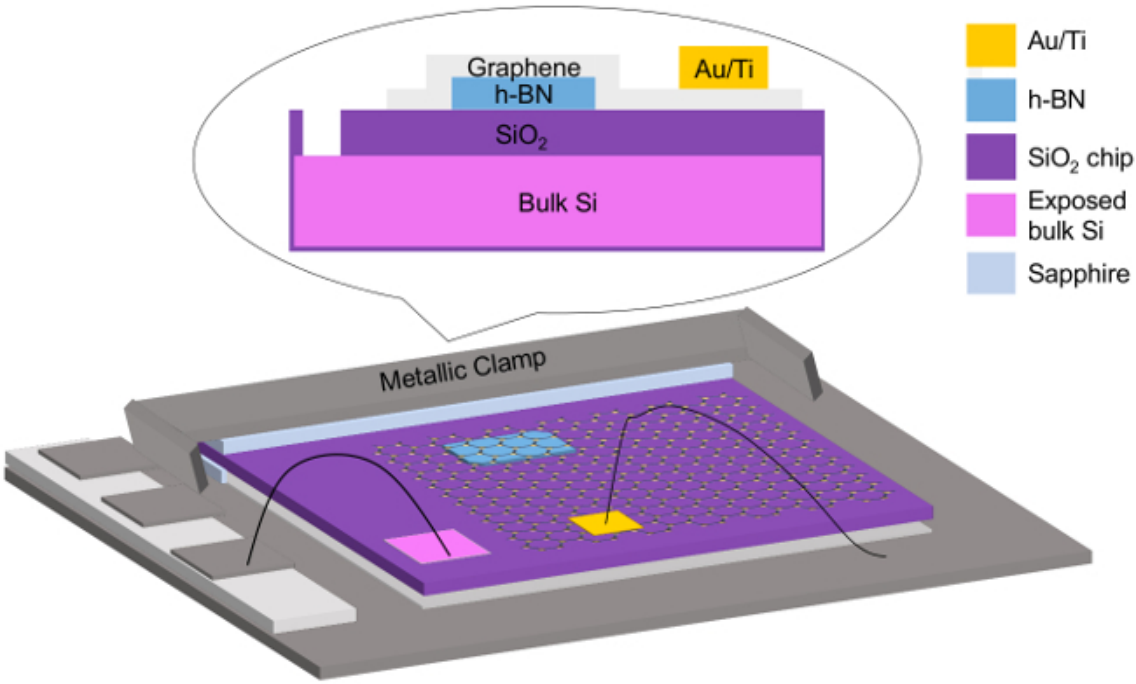

Figure 1. Schematic of a gate-tunable graphene device. Graphene is grounded to the sample plate while Si layer connects to a gate electrode through wire-bonding.[2-5] Please click here to view a larger version of this figure.

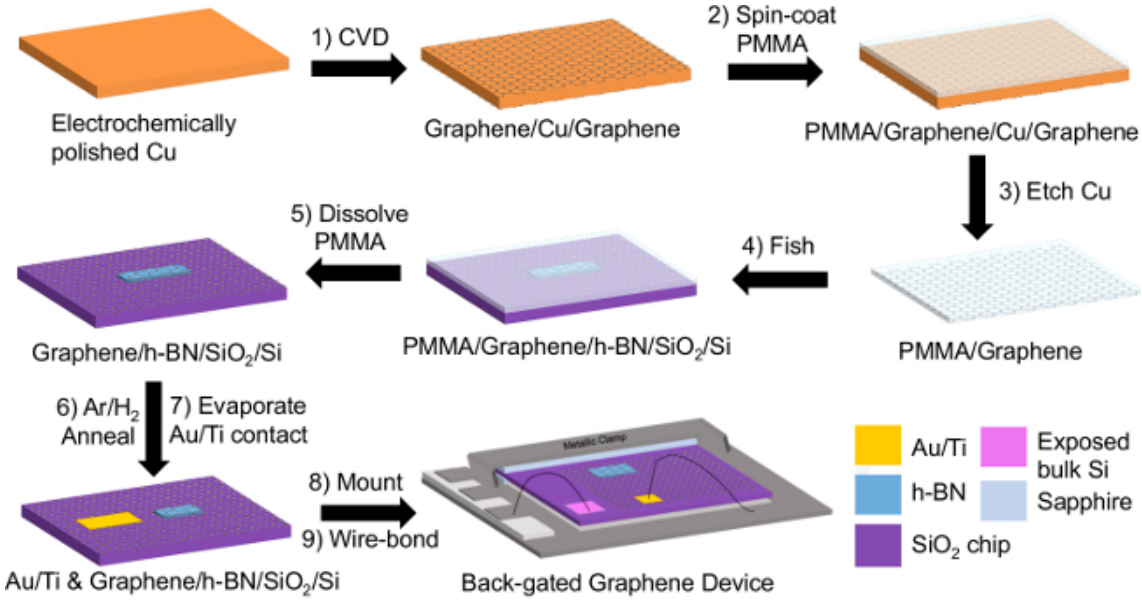

Figure 2. Process schematics of gate-tunable graphene device fabrication. The steps of fabricating a gate-tunable graphene device include: 1) CVD graphene growth on an electrochemically polished Cu foil, 2) – 5) PMMA transfer of graphene onto a h-BN/SiO_2 chip, 6) Ar/H_2 annealing, 7) evaporation of Au/Ti contact, 8) mounting onto an UHV sample plate, and 9) wire-bonding. Please click here to view a larger version of this figure.

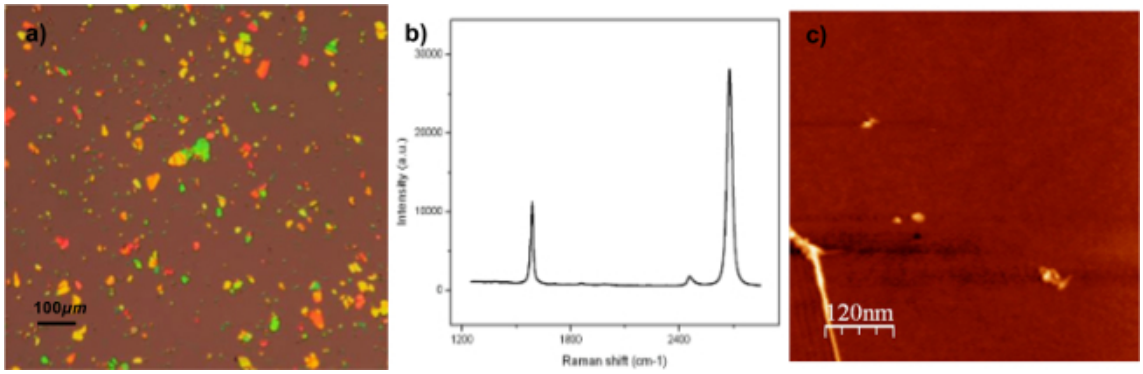

Figure 3. Pre-STM characterization of a graphene/h-BN/SiO_2 heterostructure. (A) Optical microscope image of graphene/h-BN/SiO_2 heterostructure. **(B)** Raman spectrum of graphene/SiO_2 region. Raman spectrum of graphene is characterized by D (~1,350 cm^{-1}), G (~1,580 cm^{-1}), and 2D (~2,690 cm^{-1}) peaks.[32] **(C)** Atomic force microscope (AFM) image of graphene/h-BN/SiO_2 region. This image is a height map taken with tapping mode AFM. Please click here to view a larger version of this figure.

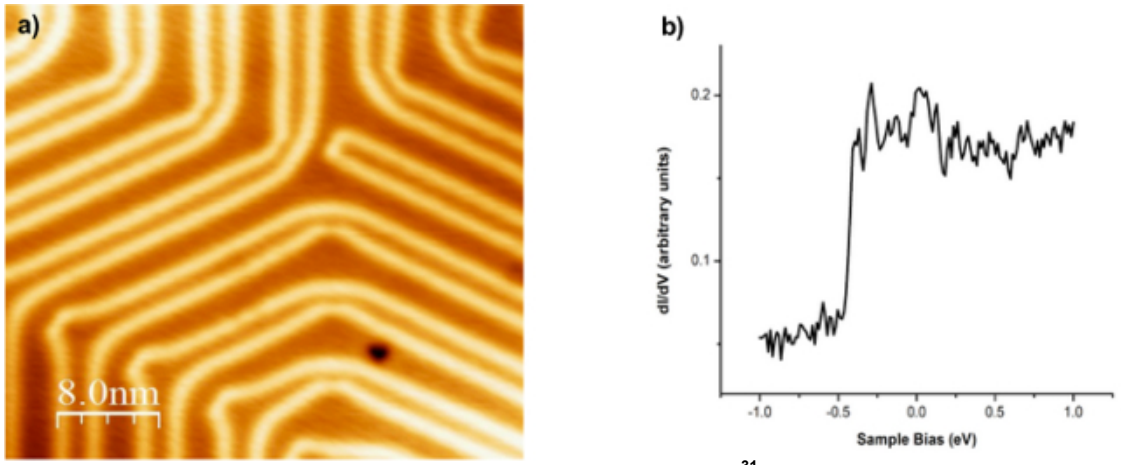

Figure 4. STM characterization of Au(111) surface for STM tip calibration.[31] **(A)** Topography of Au(111) surface. **(B)** Standard *dI/dV* spectrum of Au(111) surface. Please click here to view a larger version of this figure.

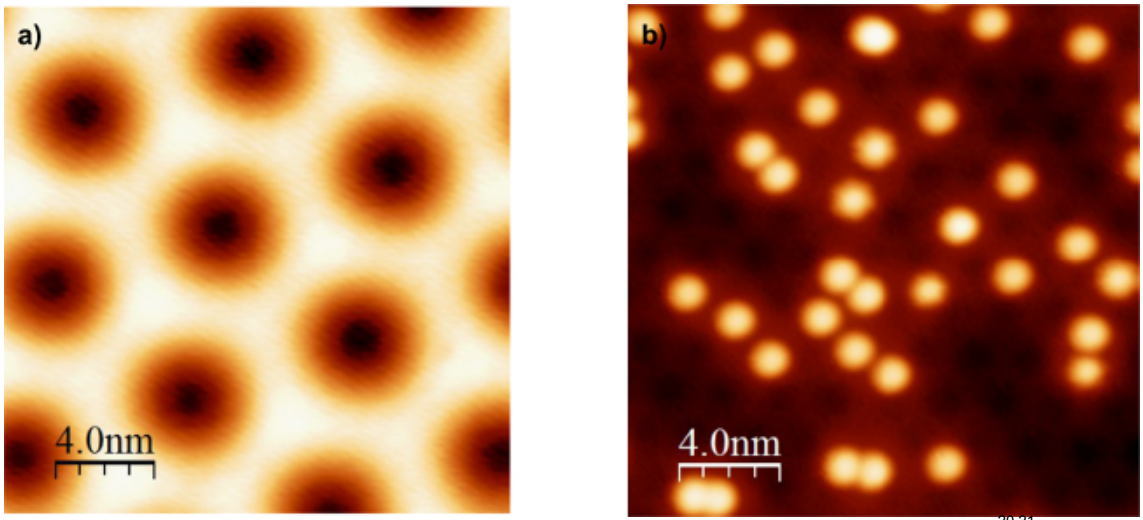

Figure 5. STM Topography of Coulomb impurities on graphene. (A) Moiré pattern for graphene/h-BN.[20,21] **(B)** Ca adatoms on graphene.[4] Please click here to view a larger version of this figure.

Discussion

For STM characterization, critical goals of the graphene device fabrication include: 1) growing monolayer graphene with a minimal number of defects, 2) obtaining a large, clean, uniform, and continuous graphene surface, 3) assembling a graphene device with high resistance between the graphene and the gate (*i.e.,* no “gate leakage”), and 4) depositing individual Coulomb impurities.

The first goal is governed by the CVD process, during which graphene grows on a Cu foil. Although there are multiple substrate candidates (*e.g.,* Ni, Ru, Ir, Pt, Co, Pd, *etc.*), Cu is well known to produce monolayer graphene most selectively due to its extremely low carbon solubility.[25] Nevertheless, selectively growing monolayer graphene can still be difficult and inconsistent due to a wide range of factors.[22-25] Although electrochemical polishing certainly provides a better substrate condition for graphene growth, our AFM characterizations have shown that the Cu surface remains non-uniform and rough on the microscopic level. Moreover, the level of contamination from chemical residue may vary from foil to foil. Annealing parameters are essential for consistently providing a clean and uniform Cu surface during growth. Annealing the Cu at a high temperature (1,050 °C) near its melting point (1,085 °C) with a high flow of hydrogen (~200 sccm) seems to provide a consistently clean and uniform Cu surface with large Cu domains.[22] The growth temperature, pressure regime, and CH_4:H_2 flow rate ratio can then be systematically optimized until monolayer graphene with a minimal number of defects is obtained.

The second goal — obtaining a large, clean, uniform, and continuous graphene surface — is governed by the PMMA transfer and Ar/H_2 annealing. Although there are a number of different graphene transfer methods (*e.g.,* dry PMMA/PDMS transfer[27], wet PDMS transfer[24], *etc.*), PMMA transfer with $FeCl_3$ (aq) etchant solution[28] has consistently yielded the most continuous/uniform graphene surfaces. However, this method leaves a high density of chemical residue on the graphene surface. To resolve this issue, the spin-coating rate and time were first optimized to make the PMMA layer as uniform as possible. Additionally, multiple cleaning steps with ultra-pure water baths were introduced to remove chemical residue from the graphene's back surface before fishing it out with an h-BN/SiO_2 chip. From these efforts, relatively clean samples, as seen by an optical microscope, have been transferred consistently. No variation in the PMMA transfer method, however, can completely clean up the graphene surface as it always leaves a thin layer of PMMA. To obtain an atomically clean surface (STM studies require clean regions >100 nm^2), a series of annealing procedures must be performed. Ar/H_2 annealing can effectively remove a majority of the PMMA layer. After Ar/H_2 annealing,[29] the graphene surface appears to be clean under inspection by ambient AFM (**Figure 3**). Yet, a thin PMMA layer undetectable by ambient AFM still covers the graphene surface, which requires further *in situ* UHV annealing to remove. It is important to keep in mind that post-transfer annealing can only clean a relatively residue-free surface only; a sample's ultimate cleanliness depends mainly on the transfer.

The third goal — assembling a graphene device without any gate leakage — is governed by post-Ar/H_2 annealing steps. When mounting the device on a sample plate, it is critical to electrically disconnect the device from the rest of the sample plate with sapphire flakes; the only electrical contact between the sample plate and the device should be the wire-bonds. Wire-bonding introduces the risk of breaking the device if excessive power is supplied as any form of fracture in the SiO_2 layer (regardless of how small) may lead to gate leakage. Wire-bonding parameters must thus be optimized ahead of time. Because gate leakage may occur not only in the device but also throughout the STM chamber, a large amount of time and resources may be wasted to identify and fix the leakage source. It is important to minimize the risk of gate leakage while assembling a graphene device.

The fourth goal — depositing individual Coulomb impurities — is governed by the calibration steps prior to the deposition. It is imperative to optimize the deposition parameters in the UHV test chamber (and additionally on the Cu(100) surface *in situ*) for a controlled deposition. Purity of the deposition needs to be carefully evaluated with an RGA because random impurities will not only skew the deposition rate measured by QCM but also result in unwanted doping. If the device were irreversibly doped by an unknown impurity, the graphene's response to Coulomb impurities might be undesirably altered.

In addition to these challenges, an STM study may be limited in several ways. In a differential conductance measurement, it is impossible to completely decouple the tip electronic states from the sample states. Even with a well-calibrated tip, it may be challenging to determine the origin of a spectroscopic feature. Moreover, information gained from measurements carried out in UHV (10^{-10} Torr) and a T = 4 K may not be relevant to devices operated in less ideal conditions.

That being said, STM has many advantages over other techniques. It has not only a high energy resolution (few meV) but also a high spatial resolution (~10 pm). For comparison, ARPES has a relatively lower spatial resolution (sub-micron), but a comparable energy resolution (few meV). STM can also be used to manipulate the position of individual atoms on a device to create novel charge configurations. For example, Yang *et al.* created artificial nuclei of charged Ca dimers on a back-gated graphene device with an STM tip and characterized an atomic collapse state on the graphene surface.[4] With these advantages in mind, STM is one of the most powerful and reliable techniques for characterizing the spatially dependent response of graphene to various perturbations in a well-controlled environment.

STM studies of gate-tunable graphene devices deposited with Coulomb impurities are valuable not only for testing fundamental theories but also for understanding hybrid graphene device applications. They can experimentally verify fundamental predictions about the behavior of massless Dirac fermions in novel systems, which exhibit significantly different behavior compared to charge carriers in conventional systems.[15-18] Furthermore, such studies can reveal some of graphene's most unexpected characteristics[4], which leads to a deeper understanding of charge carriers in relativistic regimes. New insight into the physical laws that govern graphene systems will be highly beneficial for precision tuning of the properties of hybrid graphene devices.[2-5]

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