

Video Article

Making Record-efficiency SnS Solar Cells by Thermal Evaporation and Atomic Layer Deposition

Rafael Jaramillo^{2,4}, Vera Steinmann^{1,2}, Chuanxi Yang³, Katy Hartman^{2,4}, Rupak Chakraborty^{1,2}, Jeremy R. Poindexter^{2,4}, Mariela Lizet Castillo², Roy Gordon⁵, Tonio Buonassisi^{1,2}

¹Department of Mechanical Engineering, Massachusetts Institute of Technology

²Laboratory for Manufacturing and Productivity, Massachusetts Institute of Technology

³School of Engineering and Applied Sciences, Harvard University

⁴Department of Materials Science and Engineering, Massachusetts Institute of Technology

⁵Department of Chemistry & Chemical Biology, Harvard University

Correspondence to: Rafael Jaramillo at rjaramil@mit.edu

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Abstract

Tin sulfide (SnS) is a candidate absorber material for Earth-abundant, non-toxic solar cells. SnS offers easy phase control and rapid growth by congruent thermal evaporation, and it absorbs visible light strongly. However, for a long time the record power conversion efficiency of SnS solar cells remained below 2%. Recently we demonstrated new certified record efficiencies of 4.36% using SnS deposited by atomic layer deposition, and 3.88% using thermal evaporation. Here the fabrication procedure for these record solar cells is described, and the statistical distribution of the fabrication process is reported. The standard deviation of efficiency measured on a single substrate is typically over 0.5%. All steps including substrate selection and cleaning, Mo sputtering for the rear contact (cathode), SnS deposition, annealing, surface passivation, Zn(O,S) buffer layer selection and deposition, transparent conductor (anode) deposition, and metallization are described. On each substrate we fabricate 11 individual devices, each with active area 0.25 cm². Further, a system for high throughput measurements of current-voltage curves under simulated solar light, and external quantum efficiency measurement with variable light bias is described. With this system we are able to measure full data sets on all 11 devices in an automated manner and in minimal time. These results illustrate the value of studying large sample sets, rather than focusing narrowly on the highest performing devices. Large data sets help us to distinguish and remedy individual loss mechanisms affecting our devices.

Video Link

The video component of this article can be found at <https://www.jove.com/video/52705/>

Introduction

Thin film photovoltaics (PV) continue to attract interest and significant research activity. However, the economics of the PV market are shifting rapidly and developing commercially successful thin film PV has become a more challenging prospect. Manufacturing cost advantages over wafer-based technologies can no longer be taken for granted, and improvements in both efficiency and cost must be sought on an equal footing.^{1,2} In light of this reality we have chosen to develop SnS as an absorber material for thin film PV. SnS has intrinsic practical advantages that could translate into low manufacturing cost. If high efficiencies can be demonstrated, it could be considered as a drop-in replacement for CdTe in commercial thin film PV. Here, the fabrication procedure for the recently reported record SnS solar cells is demonstrated. We focus on practical aspects such as substrate selection, deposition conditions, device layout, and measurement protocols.

SnS is composed of non-toxic, Earth-abundant and inexpensive elements (tin and sulfur). SnS is an inert and insoluble semiconducting solid (mineral name Herzenbergite) with an indirect bandgap of 1.1 eV, strong light absorption for photons with energy above 1.4 eV ($\alpha > 10^4$ cm⁻¹), and intrinsic *p*-type conductivity with carrier concentration in the range 10¹⁵ – 10¹⁷ cm⁻³.^{3–7} Importantly, SnS evaporates congruently and is phase-stable up to 600 °C.^{8,9} This means that SnS can be deposited by thermal evaporation (TE) and its high-speed cousin, closed space sublimation (CSS), as is employed in the manufacture of CdTe solar cells. It also means that SnS phase control is far simpler than for most thin film PV materials, notably including Cu(In,Ga)(S,Se)₂ (CIGS) and Cu₂ZnSnS₄ (CZTS). Therefore, cell efficiency stands as the primary barrier to commercialization of SnS PV, and SnS could be considered a drop-in replacement for CdTe once high efficiencies are demonstrated at the laboratory scale. However this efficiency barrier cannot be overstated. We estimate that the record efficiency must increase by a factor of four, from ~4% to ~15%, in order to stimulate commercial development. Developing SnS as a drop-in replacement for CdTe will also require growth of high quality SnS thin films by CSS, and the development of an *n*-type partner material on which SnS can be grown directly.

Below is described the step-by-step procedure for fabricating record SnS solar cells using two different deposition techniques, atomic layer deposition (ALD) and TE. ALD is a slow growth method but to-date has yielded the highest efficiency devices. TE is faster and industrially

scalable, but lags ALD in efficiency. In addition to the different SnS deposition methods, the TE and ALD solar cells differ slightly in the annealing, surface passivation, and metallization steps. The device fabrication steps are enumerated in **Figure 1**.

After describing the procedure, test results for the certified record devices and related samples are presented. The record results have been reported previously. Here the focus is on the distribution of results for a typical processing run.

Protocol

1. Substrate Selection and Cutting

1. Purchase polished Si wafers with a thick thermal oxide. For the devices reported here, use 500 μm thick wafers with a 300 nm or thicker thermal oxide. The substrate selection criteria are discussed in the Discussion section.
2. Spin coat the polished side of wafer with a typical positive photoresist (SPR 700 or PMMA A. 495) and soft bake (30 sec at 100 °C).
Note: This is a protective layer to prevent damage or contamination during the subsequent cutting step.
3. Use a die saw to cut the wafer into 1" $\times$ 1" (25.4 $\times$ 25.4 mm²) square substrates.

2. Substrate Cleaning

1. Remove particulates and other residue that result from cutting step using a compressed nitrogen gun, followed by an ultrasonic bath in de-ionized (DI) water for 5 min at 45 – 60 °C.
2. Remove the photoresist layer with an ultrasonic bath in acetone for 5 min at 45 – 60 °C.
3. Clean the exposed substrate with 3 subsequent ultrasonic baths, all for 5 min at 45 – 60 °C: acetone, ethanol, and isopropyl alcohol. Finish by drying with a compressed nitrogen gun, while substrates remain in the quartz carrier.

3. Mo Sputtering

1. Load the clean Si / SiO₂ substrates into a high vacuum sputtering system. Ensure that the substrate plate is unheated and substrate rotation is enabled. For the devices reported here, process in a commercial system with tilted magnetron guns with 2" targets and a throw distance of approximately 4".
2. Deposit the first layer (the adhesion layer) at relatively high background pressure such as 10 mTorr of Ar. For the devices reported here, process with a sputtering power of 180 W (DC), which gives a growth rate of 2.6 Å/sec, and a first Mo layer that is 360 nm thick.
3. Deposit the second layer (the conductive layer) at a relatively low background pressure such as 2 mTorr of Ar. Use the same sputtering power as the first layer (180 W) and deposit the same thickness.
Note: The devices reported here had a second Mo layer that was 360 nm thick, same as the first layer.
4. After Mo deposition, store the substrates under vacuum until the SnS deposition step.

4. SnS Deposition

Note: The ALD deposition technique is described in sub-section 4.1, and the TE deposition is described in sub-section 4.2. The ALD deposition system is shown in **Figure 2**, and TE deposition system is shown in **Figure 3**.

1. Deposit SnS by ALD
 1. Before loading into the reactor, put Mo substrates in a UV ozone cleaner for 5 min to remove organic particles. Then place the substrates on the substrate holder and insert into the deposition zone.
 2. Stabilize the furnace temperature at 200 °C before starting deposition.
 3. Grow SnS thin films from the reaction of bis(*N,N'*-diisopropylacetamidinato)-tin(II) [Sn(MeC(*N*-iPr)₂)₂, referred to here as Sn(amd)₂] and hydrogen sulfide (H₂S)⁴.
 1. Keep the Sn(amd)₂ precursor at a constant temperature of 95 °C. Use pure N₂ gas to assist the delivery of Sn(amd)₂ vapor from the container in the oven to the deposition zone. During each ALD cycle, supply three doses of Sn(amd)₂ precursor for total exposure of 1.1 Torr second.
 2. Use a gas mixture of 4% H₂S in N₂ as the sulfur source. Ensure that the exposure to the hydrogen sulfide vapor is 1.5 Torr second per dose. Ensure that the partial pressure of H₂S and the total pressure of H₂S in N₂ are 0.76 Torr and 19 Torr, respectively.
 4. Set the pumping time between Sn precursor dose and H₂S dose to be only 1 sec (short compared to most other conventional ALD procedures) in order to speed up the deposition.
Note: Because the Sn precursor is not completely removed by this short pumping time, some residual Sn precursor remains when the H₂S arrives. Thus the process could be described as a pulsed CVD process. The growth rate of SnS film is 0.33 Å/cycle, or 0.04 Å/sec.
2. Deposit SnS by TE
 1. Ensure that the process chamber pressure is 2 $\times$ 10⁻⁷ Torr or lower. Load substrates into the chamber through the load lock. Hold the substrates to the plate either with a single clip, or with a custom substrate holder with appropriately sized pockets that is screwed down to the substrate plate.
 2. Ramp the source and substrate heaters to their setpoints. For the device reported here the substrate temperature is 240 °C and the growth rate is 1 Å/sec; to achieve this growth rate set the source temperature in the range 550 – 610 °C (the required source temperature increases with time for a single load of source powder). The target film thickness is 1,000 nm.

3. Measure deposition rate using the quartz crystal monitor (QCM) before and after the SnS film deposition by moving the QCM arm into the process chamber. For this measurement the substrate is raised so that the QCM can be moved into the substrate growth position. Note: The deposition rate remains fairly constant throughout a deposition time of 3 hr (± 0.05 Å/sec deviation).
4. After deposition, transfer the samples back into the load lock before venting to air. Quickly transport the samples through air into storage either in vacuum or in an inert atmosphere glovebox before the next processing step. Note: The typical unintentional air exposure time is approximately 3 min. The typical storage time is between a day and a week.

5. SnS Annealing

Note: This step is performed slightly differently for ALD and TE solar cells. The annealing procedure for ALD solar cells is described in sub-section 5.1, and the procedure for TE solar cells is described in sub-section 5.2. The purpose of annealing is discussed in the Discussion section.

1. Anneal the ALD-grown SnS films in H₂S gas.
Note: This step is performed in the same system used for ALD growth.
 1. Use pure H₂S gas (99.5% pure) at a flow rate of 40 sccm and pressure of 10 Torr.
 2. Heat the SnS film to a temperature of 400 °C and hold for 1 hr in the H₂S gas environment. Ensure that the gas is flowing throughout the whole process, including temperature ramping up and down.
2. Anneal the TE-grown SnS films in H₂S gas. Perform this step in a dedicated tube furnace.
 1. Load the samples onto a clean quartz plate and slide into the hot-zone region of the furnace.
 2. After the furnace is sealed, purge three times with pure N₂ and allow to pump down to base pressure.
 3. Establish gas flow at 100 sccm of 4% H₂S at 28 Torr.
 4. Ramp the temperature to 400 °C over 10 min. Hold at 400 °C for 1 hr, then allow the samples to cool unassisted in the hot-zone. Maintain constant H₂S gas flow and pressure until samples cool below 60 °C. Remove the samples and either proceed immediately to the next step, or place them into storage in an inert gas glove box.

6. SnS Surface Passivation with a Native Oxide

Note: This step is performed slightly differently for ALD and TE solar cells. In sub-section 6.1 the surface passivation procedure for ALD solar cells is described, and the procedure for TE solar cells is described in sub-section 6.2. The function of this step is further discussed in the Discussion section.

1. For the ALD-grown samples, grow a thin layer of SnO₂ by ALD.
Note: We use a different reactor than that used for SnS growth.
 1. Grow SnO₂ by the reaction of cyclic amide of tin [(1,3-bis(1,1-dimethylethyl)-4,5-dimethyl-(4R,5R)-1,3,2-diazastannolidin-2-ylidene)Sn(II)] and hydrogen peroxide (H₂O₂). Store the cyclic amide tin precursor in an oven at 43 °C, and the H₂O₂ in a bubbler at RT.
 2. Maintain substrate temperature at 120 °C for deposition.
 3. Expose the tin precursor and H₂O₂ using 0.33 and 1.5 Torr second per cycle, respectively, for a total of 5 cycles. Check that the thickness of the resulting SnO₂ is 0.6–0.7 nm, as measured by X-ray photoelectron spectroscopy (XPS) analysis¹⁰.
2. For the TE-grown samples, form a thin layer of SnO₂ by air exposure.
 1. Expose the samples to lab ambient air for 24 hr. Check that the thickness of the resulting SnO₂ is approximately 0.5 nm, as measured by XPS analysis.
Note: The typical RT is 24 ± 1 °C, and the typical humidity is 45% ± 13% (higher in the summer); for the devices reported here, the values were 24.6 °C and < 30%, respectively.

7. Deposition of the Zn(O,S) / ZnO Buffer Layer

Note: This step is performed in the same ALD chamber that is used for SnS growth by ALD.

1. Grow a Zn(O,S):N layer by ALD.
 1. Maintain the substrate temperature at 120 °C.
 2. Grow Zn(O,S):N by ALD from the reaction of diethylzinc (Zn(C₂H₅)₂, DEZ), deionized water (H₂O), 4% H₂S in N₂, and ammonia (NH₃)¹¹. Store the bubbler containing DEZ at RT. Use a cycle sequence of [DEZ-H₂O-DEZ-NH₃]₁₄-[DEZ-H₂S]₁, and repeat this super cycle 12 times. Ensure that the exposure of ammonia is 11 Torr second.
 3. Check that the S/Zn ratio in the resulting film is 0.14, as measured by Rutherford backscattering spectroscopy¹², and that the thickness of the film is approximately 36 nm.
2. Grow a ZnO layer by ALD.
 1. Maintain the substrate temperature at 120 °C.
 2. Grow ZnO with 50 ALD cycles of DEZ-H₂O.
Note: The thickness of the resulting ZnO film is approximately 18 nm.

8. Deposition of the Transparent Conducting Oxide (TCO), Indium Tin Oxide (ITO)

1. Cut ITO shadow masks from a 0.024" (610 μm) aluminum 6061 sheet using a laboratory laser cutter.
Note: The masks define 11 rectangular devices that are 0.25 cm^2 in size plus a larger pad in one corner that is used for optical reflectivity measurements, see **Figure 4**.
2. Mount the devices and masks in a mask aligner.
Note: This is an aluminum plate with nested pockets for the substrate and masks and clips to secure the masks in place.
3. Deposit ITO by reactive magnetron sputtering.
 1. Heat the substrate to approximately 80 – 90 °C and enable substrate rotation.
 2. Use a 2 inch diameter ITO target ($\text{In}_2\text{O}_3/\text{SnO}_2$ 90/10 wt.%, 99.99% pure) at 65 W RF sputtering power with 40 / 0.1 sccm Ar / O_2 gas flow at 4 mTorr total pressure.
 3. Grow a 240 nm thick ITO film.
 Note: With these parameters, growth rates of 0.5 Å/sec and sheet resistances in the range 40 – 60 Ω/sq are achieved.

9. Metallization

1. Cut metallization shadow masks from a 127 μm thick austenitic stainless steel sheet.
Note: These masks are cut with +10/-5 μm tolerance by a commercial company. The metal pattern consists of 2 fingers separated by 1.5 mm, each 7 mm long, and a 1 x 1 mm^2 contact pad, see **Figure 4**.
2. Mount the devices and masks in a mask aligner, as in Step 8.2.
3. Deposit Ag (for TE devices) or Ni/Al (for ALD devices) by electron-beam evaporation.
 1. Mount mask aligner onto the substrate plate of an electron beam metals evaporation system. Pump down to a base pressure below 1 x 10⁻⁶ Torr.
 2. Evaporate metal at a rate of 2 Å/sec. Deposit 500 nm total metal thickness.

10. Device Characterization

1. Perform current-voltage ("J-V") measurements on all devices in the dark and in AM1.5 simulated solar light.
 1. Calibrate the solar simulator by collecting J-V data from a calibrated silicon solar cell and adjusting the solar simulator lamp power and height until reaching the calibrated current value for AM1.5 insolation.
 2. Contact the devices in four-wire mode by using copper beryllium double probe tips to contact to both the top (anode, Ag or Al) and bottom (cathode, Mo) layers. Contact the bottom layer by scratching away the buffer and SnS layers with a scalpel blade.
 3. Measure light and dark J-V data using a source-meter by sourcing voltage and measuring current.
Note: Devices are typically measured within the range ± 0.5 V. The devices are not responsive to the direction or rate of the voltage sweeps. For routine testing an area-defining light aperture is not used, see Discussion section for further details.
2. Perform external quantum efficiency (EQE) measurements on all devices, with variable light and voltage bias.
 1. Calibrate the EQE system by measuring the response of a Si calibration photodiode.
Note: The software compares this data to measurements performed with a NIST-backed standard to adjust the light level accordingly.
 2. Contact the devices using the four-wire method, as in step 10.1.2.
 3. Measure EQE using a commercial system which illuminates the sample with monochromatic light chopped at 100 Hz over a wavelength range of 270–1,100 nm and measures the resulting current. Perform this measurement according to the manufacturer's standard operating procedure.
 4. Repeat the EQE measurement with variable voltage and white light bias. Use a sourcemeter to supply the voltage bias, and a halogen lamp to supply the light bias. Measure devices in both forward and reverse voltage bias, and under variable white light intensity up to ~1 Suns.
 5. Measure optical reflectance (%R) of the ITO top surface using a spectrophotometer with an integrating sphere in order to convert external to internal quantum efficiency (IQE). Perform this measurement according to the manufacturer's standard operating procedure.

Representative Results

In **Figures 6-8** results are shown for two representative "baseline" TE-grown samples as described above. Illuminated J-V data for these two samples is plotted in **Figure 6**. The first sample ("SnS140203F") yielded the device with certified efficiency of 3.88% that was reported previously.⁹ Representative J-V distributions are also shown for each sample. For a given bias voltage, these distributions are calculated as $\langle J \rangle \pm \sigma_J / \sqrt{N}$ where $\langle J \rangle$ is the average of the current density measured for all devices, σ_J is the standard deviation of these measurements, and N is the total number of measurements. In other words, the average and the standard error are graphically represented. This representation helps with comparing results from different samples, and for visually assessing the impact of changes in device fabrication on the resulting device performance.

The J-V data suggest that the samples suffer from problems with shunt resistance that varies between devices on a sample. This conclusion is further reinforced by **Figures 7 and 8**. In **Figure 7** the standard solar cell parameters are plotted — open circuit voltage (V_{OC}), short circuit current density (J_{SC}), fill factor (FF), and power conversion efficiency — for all the same devices shown in **Figure 6**. The bar graph representation helps to visually identify correlations between parameters. For these samples the most apparent correlation is between efficiency

and the FF, as expected for devices that suffer from shunt or series resistance losses. For the second device there is also an apparent correlation between efficiency and V_{OC} , as expected for shunt resistance losses.

These correlations are made explicit by the multivariate plots shown in **Figure 8**. Here, V_{OC} , J_{SC} , and FF are plotted against the series (R_s) and shunt (R_{sh}) resistances. R_s and R_{sh} are calculated using linear fits to the J - V data near 0.5 and 0 V, respectively. In many cases it would be better to extract R_s and R_{sh} as parameters in a diode model which can be fit to the J - V data. However, for relatively low efficiency solar cells there are many sources of loss, and diode models that succeed for higher efficiency devices are not reliable. Therefore it is preferred to extract R_s and R_{sh} by a more robust technique. Although the resulting values may not be accurate, the trends are still instructive and can be used to guide development. The data in **Figure 8** confirm that shunt resistance is a major source of loss. This can be seen most clearly in the rising trend in FF (R_{sh}). The data show that, at the present stage of device development, the shunt resistance must be maintained greater than approximately 200 $\Omega \text{ cm}^2$ in order for efficiency gains from other process improvements to become apparent. R_s appears not to limit the devices reported here. The values for R_s are typically 0.5 $\Omega \text{ cm}^2$, and only rarely venture above 1 $\Omega \text{ cm}^2$.

Results for one representative “baseline” ALD-grown sample as described above are shown in **Figure 9**. The ALD devices show better performance than the TE devices, with the best device showing 4.6% efficiency. Besides the different SnS growth techniques, the two fabrication procedures differ in the SnS surface passivation by oxidation. In addition, the TE samples are exposed to laboratory air in between film growth and annealing, while the ALD samples are annealed in the growth chamber without an air break. The ALD-grown samples appear to suffer less from shunt resistance losses than the TE-grown samples. The reason for this difference is not known. It is possible that the ALD-grown SnS films are more compact, due to the self-limiting growth mode and slow growth rate, than the TE-grown films.

The certified device tests are reproduced in **Figure 10**.^{9,10} On the left is shown the certified record device using an ALD-grown SnS layer. The certified efficiency for this sample was 4.36%, and devices up to 4.54% efficient have been measured using the same fabrication procedure. On the right is shown the certified record device using a TE-grown SnS layer. The certified efficiency for this sample was 3.88%, and devices up to 4.1% have been measured with the same procedure. Note that the 3.88% certified test result is well within the range measured for the same sample, for which the average $\pm$ standard deviation is 3.5% $\pm$ 0.4%, as shown in **Figure 7**.

Figure 11 shows results demonstrating the stability of TE-grown SnS solar cells in ambient conditions. For select samples J - V tests were performed before and after storing for up to eleven months. The samples were stored in air and exposed to ambient light without encapsulation. All four samples shown in **Figure 11** were processed slightly differently than the procedure reported here; this is for historical reasons, and there is no reason to think that the devices reported here would have different stability characteristics. The processing differences are described in the figure caption, and they account for the varying performance of the devices. The main point is that minimal degradation is observed over a year. It remains to be seen how SnS solar cells would survive more accelerated lifetime testing, such as damp heat or prolonged full spectrum illumination.

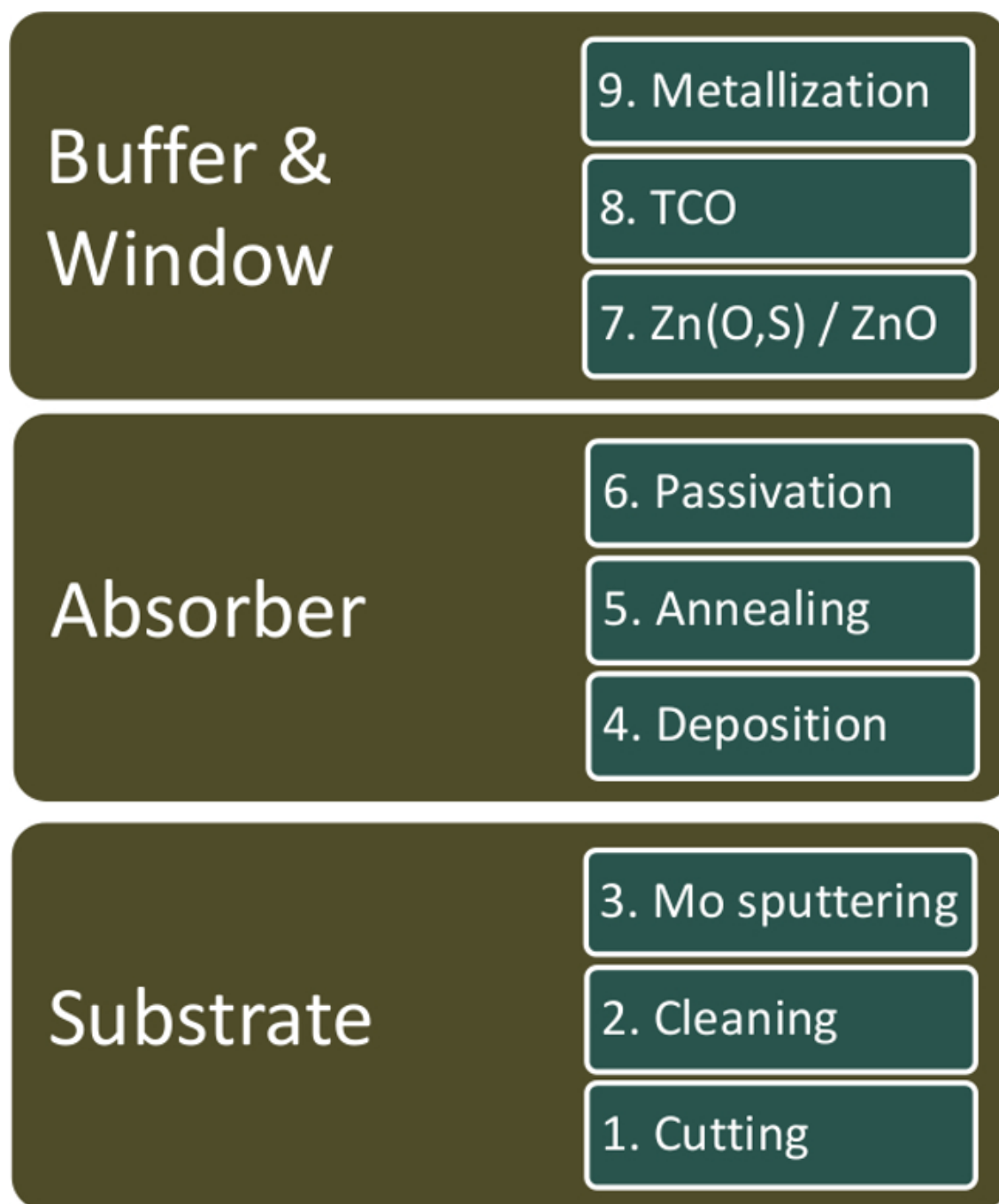
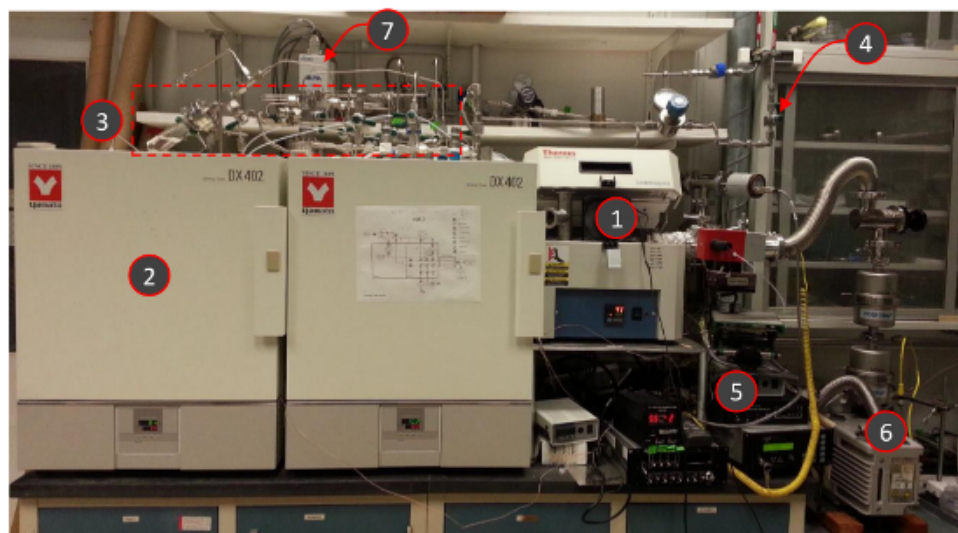
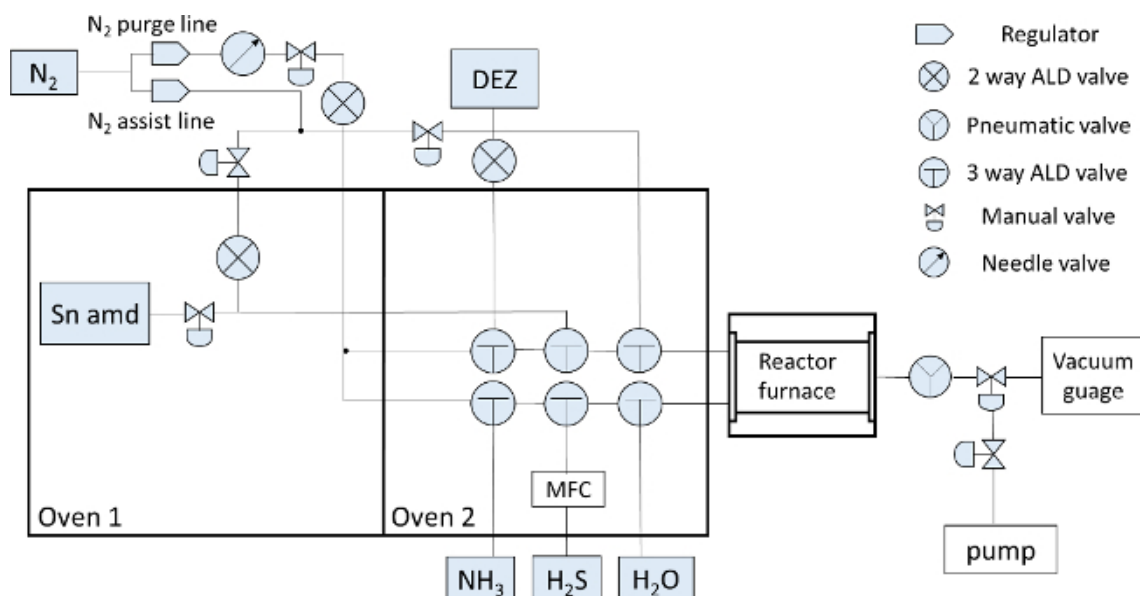
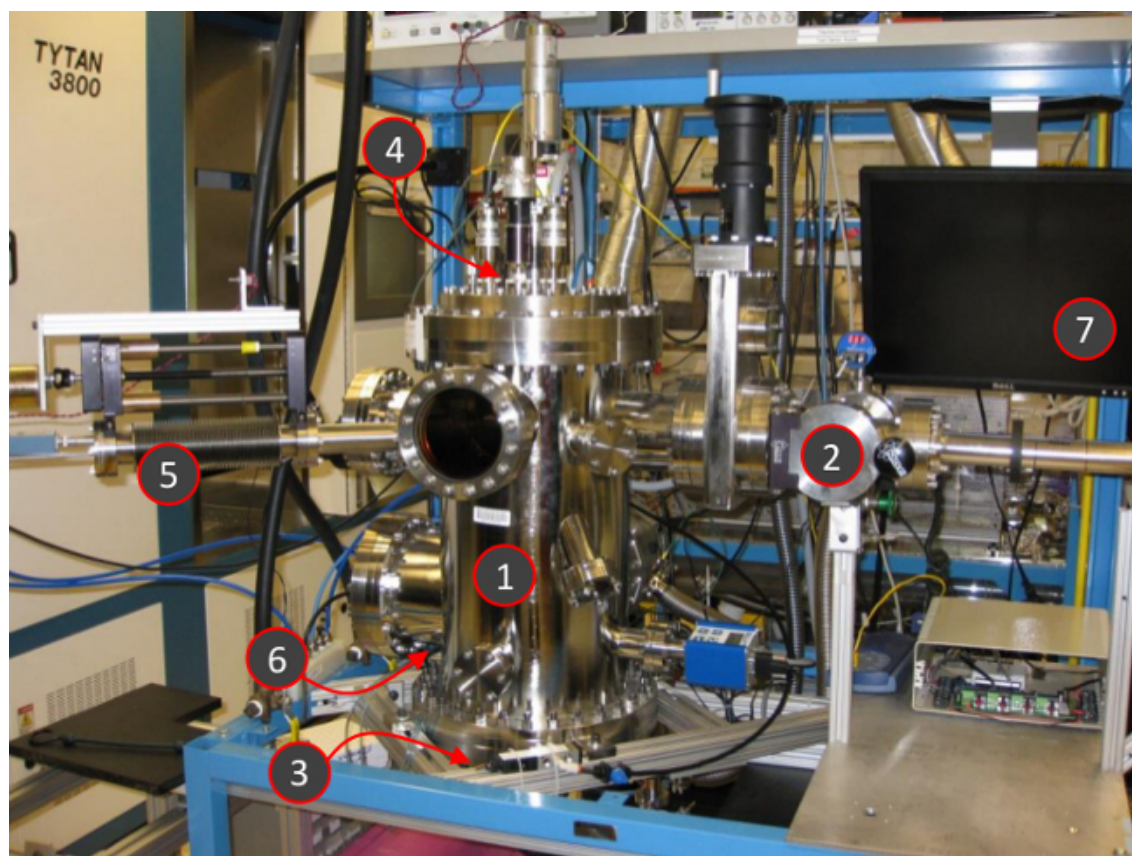


Figure 1. Device fabrication process. Enumeration of the device fabrication process, from substrate cutting (#1, bottom) to metallization (#9, top).



- | | |
|---------------------------------------|--------------------------------------|
| 1. ALD chamber | 5. Temperature controlling component |
| 2. High-temperature precursor oven | 6. pump |
| 3. Room temperature precursor sources | 7. Mass flow controller |
| 4. H2S gas pipeline | |

Figure 2. Atomic layer deposition (ALD) system overview. (Top) ALD system schematic drawing. (Bottom) ALD system photograph, with critical components numbered and labeled. This system can perform SnS deposition, SnS annealing, and buffer layer deposition and sits in the Gordon group at Harvard University. It consists of a hot-wall deposition tube, two ovens used to store precursor, gas deliver and control system, temperature controlling system and a rotary vane mechanical vacuum pump. The substrate holder can put at most eight 1" × 1" square substrates. [Please click here to view a larger version of this figure.](#)



- | | |
|------------------------------------|---|
| 1. Deposition chamber | 5. Quartz crystal monitor, on retractable arm |
| 2. Load lock chamber | 6. Pyrometer (not visible) |
| 3. Source (on bottom flange) | 7. Computer control & monitoring |
| 4. Substrate stage (on top flange) | |

Figure 3. Thermal evaporation (TE) system overview. Critical components are numbered and labeled. This system is dedicated to SnS deposition and sits in the Buonassisi group at MIT. The system consists of a process chamber and a load lock. The process chamber is typically kept under high vacuum conditions (1×10^{-8} Torr) and includes a shuttered substrate stage with sample rotation and radiative heating, and a shuttered effusion cell for source evaporation. The chamber also has a retractable quartz crystal monitor (QCM) located directly underneath the substrate plate to measure growth rate, and a pyrometer to measure substrate temperature. Commercially purchased SnS powder is used for the precursor, with a thermal pre-treatment described previously.⁹ The substrate plate holds one large device substrate (1×1 in²) and one smaller substrate ($1 \times 1/3$ in²) which is used for SnS film measurements. The distance from the substrate to the source orifice is 10 cm. [Please click here to view a larger version of this figure.](#)

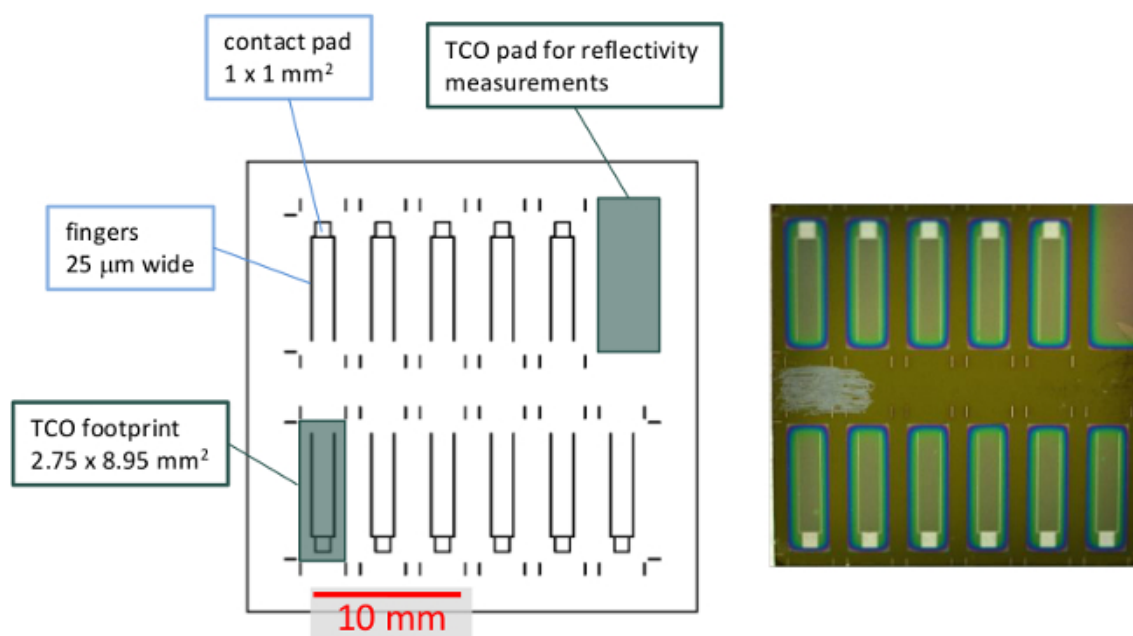


Figure 4. Metallization pattern and sample photograph. The drawing at left shows the metallization pattern for 0.25 cm^2 devices. For clarity the TCO footprint is outlined on only one device. Also shown is the location of the larger TCO pad that is used for optical reflectivity measurements. The photograph at right shows a real sample with TE-grown SnS. The scratched region at the left provides contact to the underlying Mo layer for testing. Photograph: KJ Wang. [Please click here to view a larger version of this figure.](#)

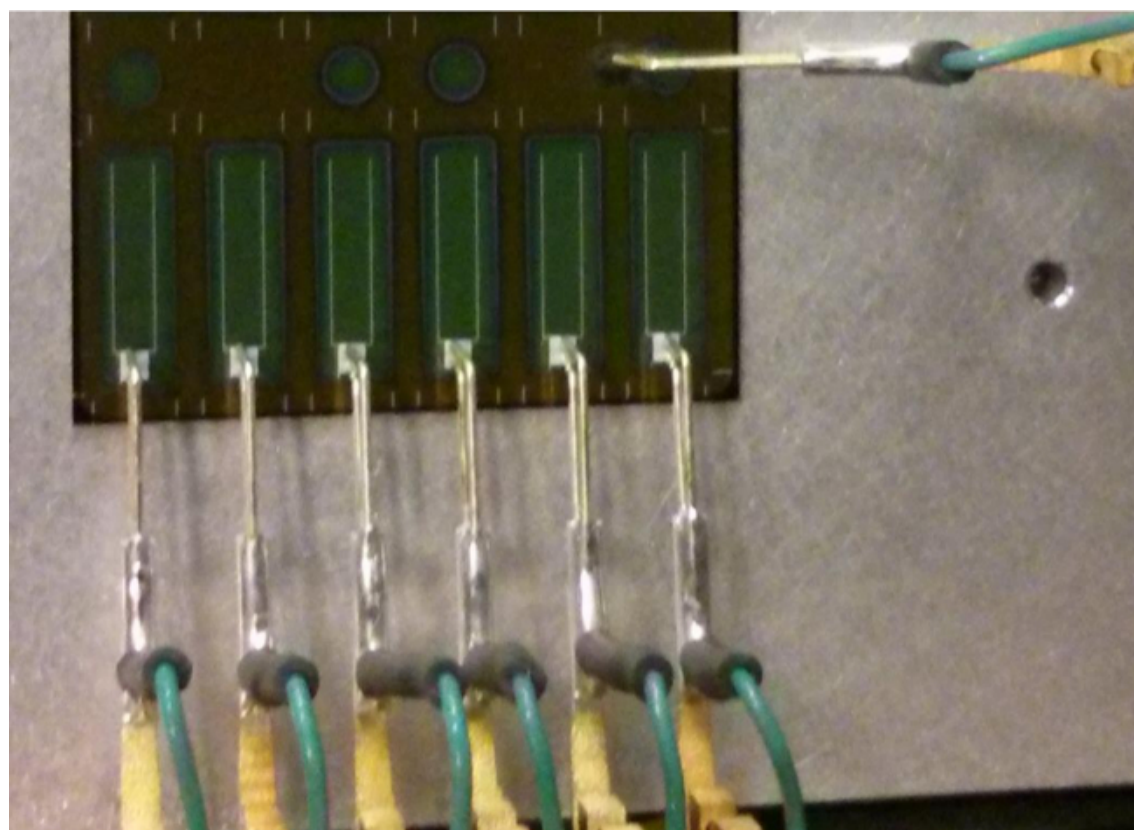


Figure 5. Device testing with probe card. This top-down image shows a sample mounted on the test station chuck with multiple devices contacted simultaneously with the custom probe card. Only half of the sample is visible in this image. [Please click here to view a larger version of this figure.](#)

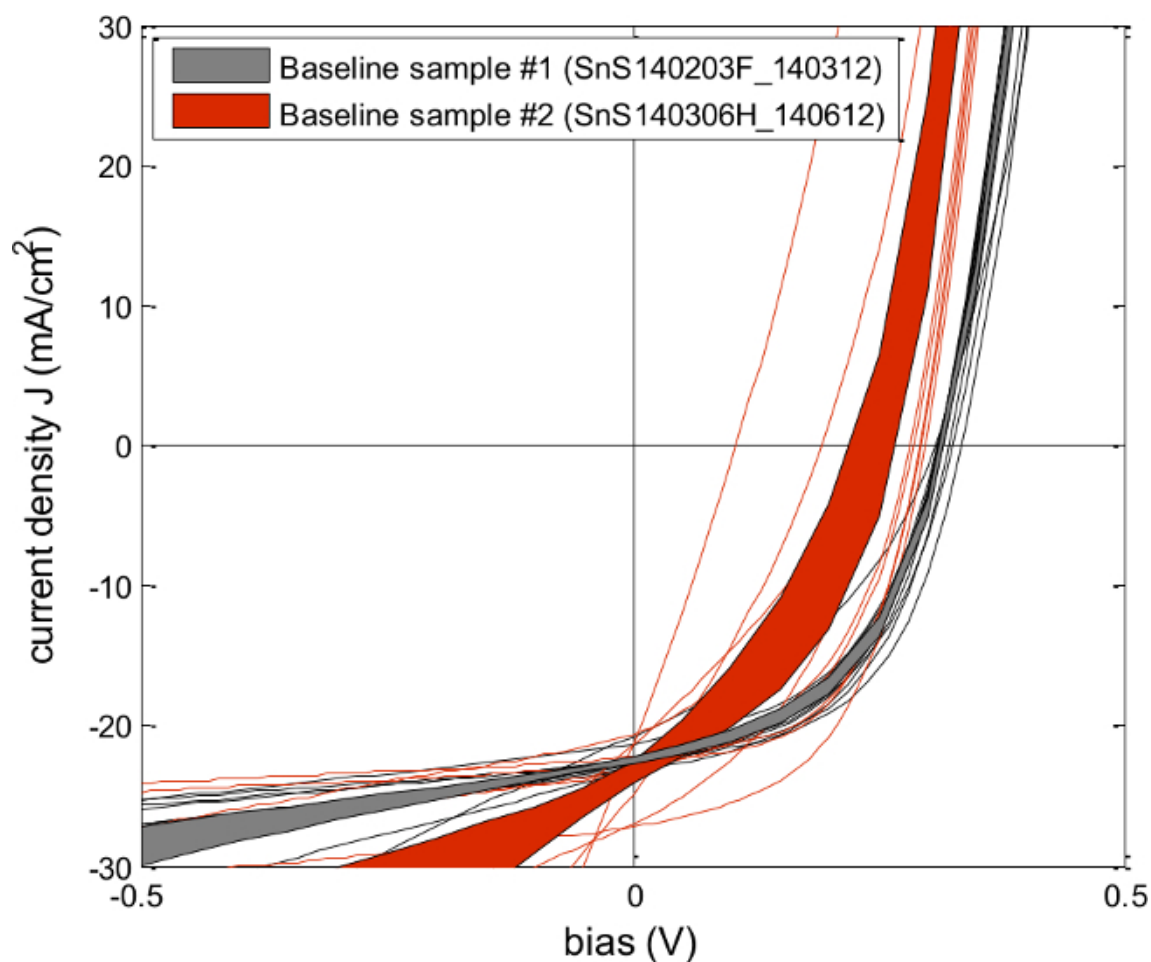


Figure 6. J-V tests for devices on two different “baseline” TE samples. For clarity, all 12 devices on a given sample are plotted in the same color (grey or red). Also plotted are representative J-V envelopes (average $\pm$ standard error) for all devices on each sample, as described in the text. These measurements were performed without an area-defining light aperture. [Please click here to view a larger version of this figure.](#)

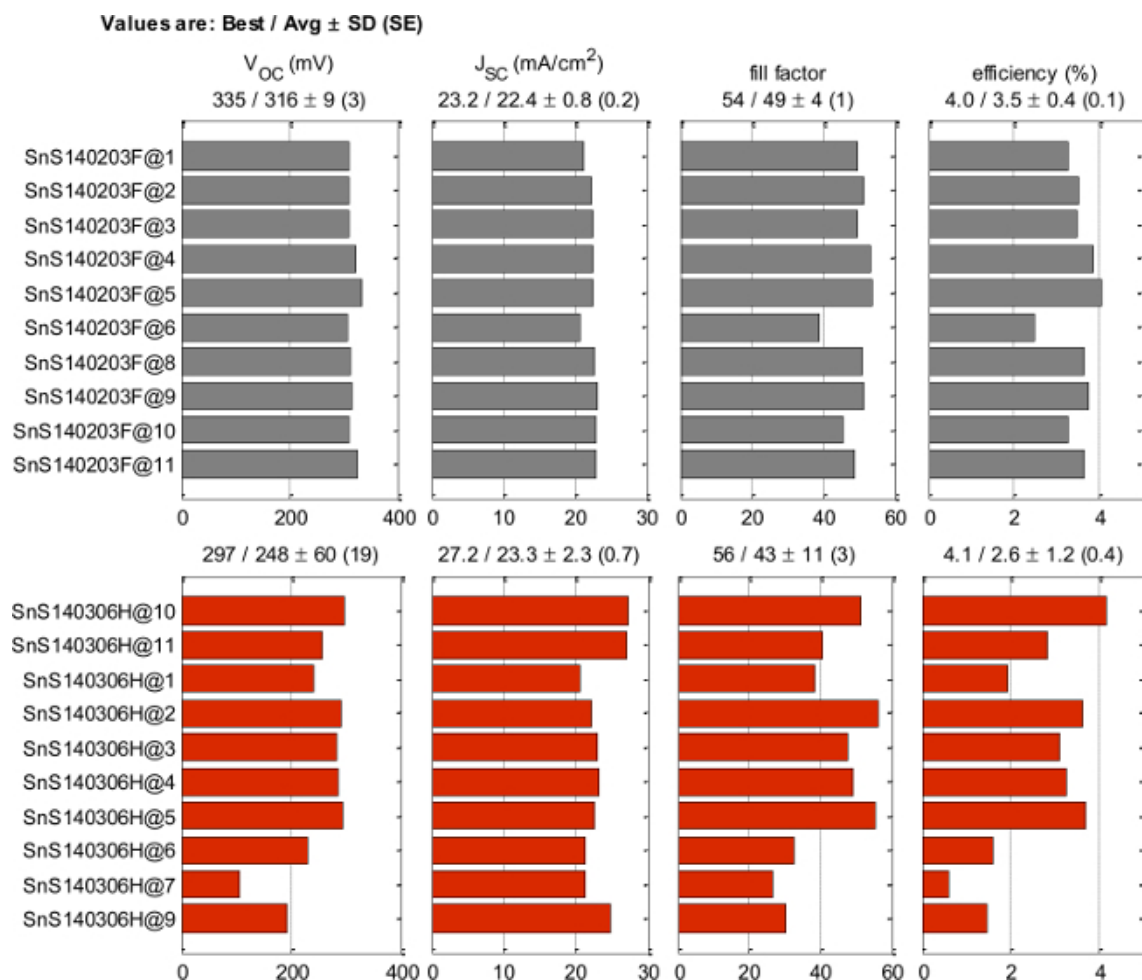


Figure 7. Solar cell test parameters for two baseline TE samples. The test results are plotted on a single line for each device tested — 11 devices each for “SnS140203F” (top) and “SnS140306H” (bottom) — to make correlations more apparent. Above each plot is reported the best, average, standard deviation (SD), and standard error (SE) for each distribution. Note that the best V_{oc} (for example) is the highest measured V_{oc} , not the V_{oc} of the most efficient device. These measurements were performed without an area-defining light aperture. [Please click here to view a larger version of this figure.](#)

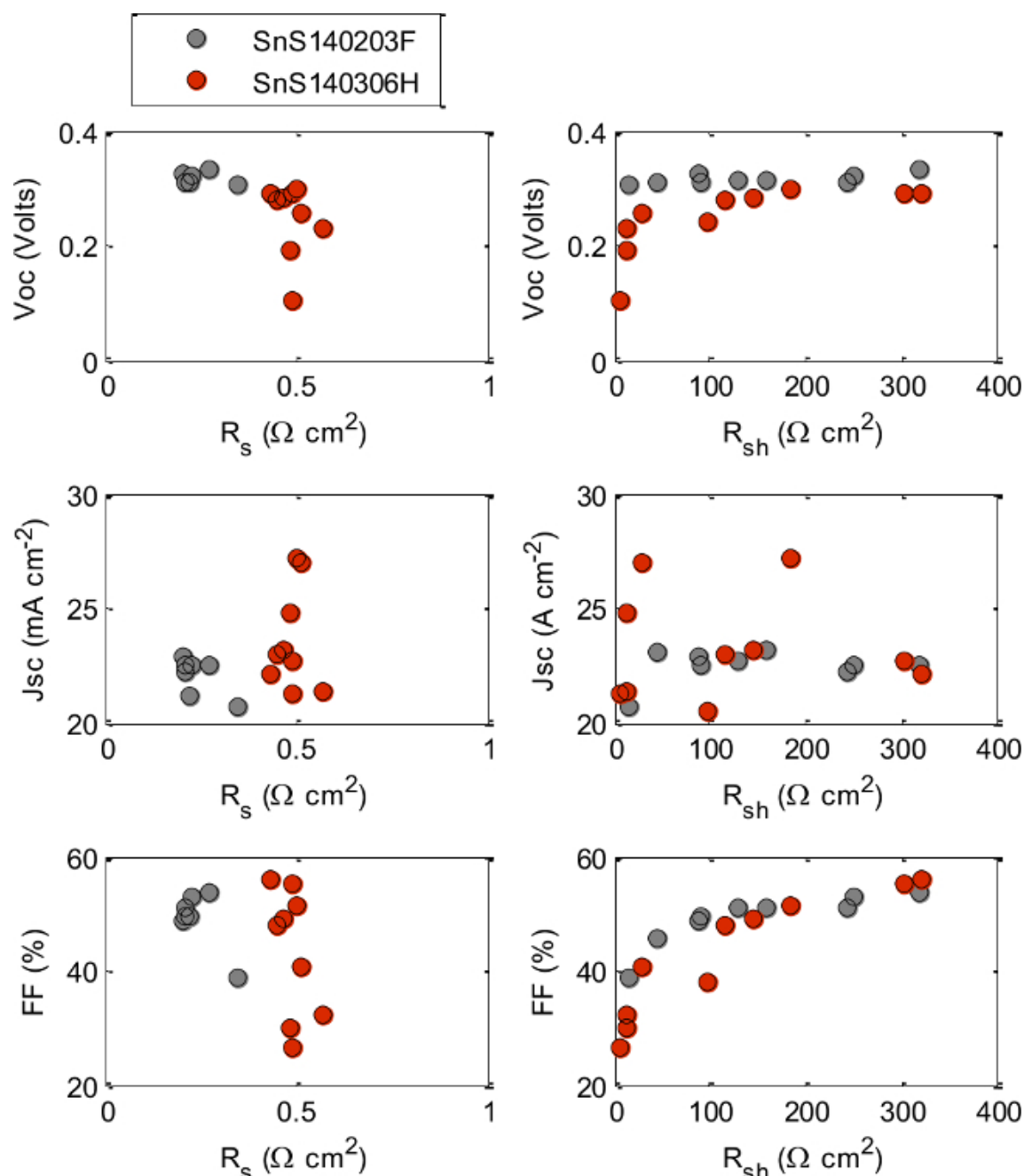
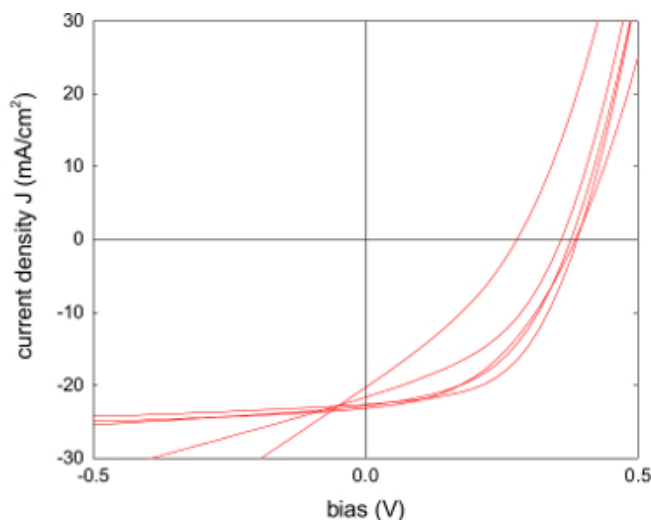


Figure 8. Series and shunt resistance multivariate plots for two baseline TE samples. The devices represented are the same reported in **Figures 6-7**. The series (R_s) and shunt (R_{sh}) resistances are calculated as described in the text. [Please click here to view a larger version of this figure.](#)



Values are: Best / Avg $\pm$ SD (SE)

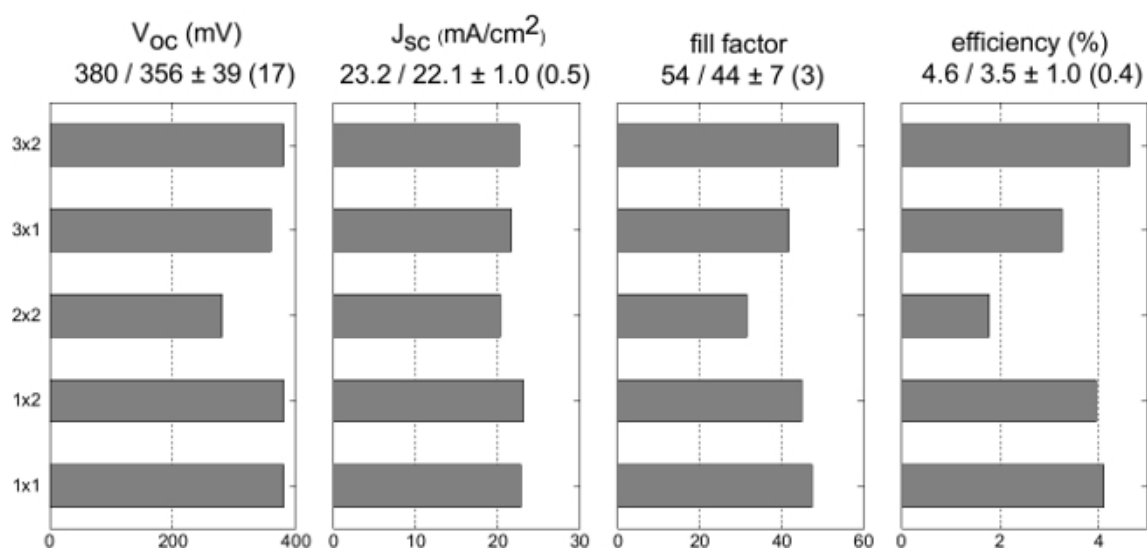


Figure 9. J-V tests and test parameters for one baseline ALD sample. (Top) The J-V curves show good peak performance, but some devices clearly suffer from low shunt resistance. (Bottom) The test parameters show a strong correlation between efficiency and the FF, consistent with shunt resistance losses. These measurements were performed without an area-defining light aperture. [Please click here to view a larger version of this figure.](#)

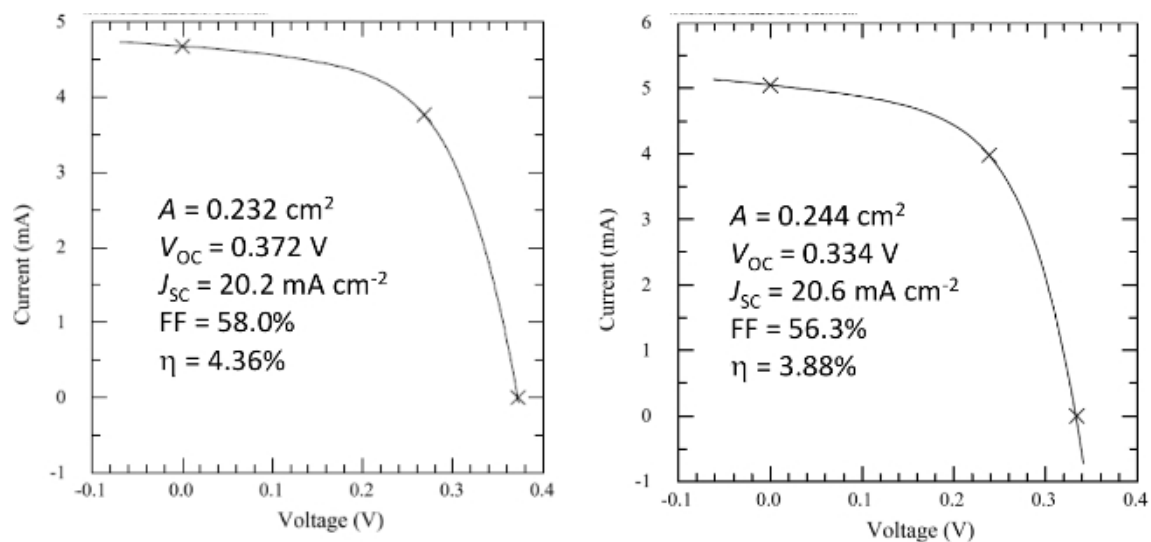


Figure 10. Certification results for ALD- and TE-grown devices. Certification performed by the PV Performance Characterization Team at the National Renewable Energy Laboratory, USA. (Left) The ALD certified record is 4.36%, as reported in Sinsermsuksakul *et al.*¹⁰ (Right) The TE certified record is 3.88%, as reported in Steinmann *et al.*⁹ [Please click here to view a larger version of this figure.](#)

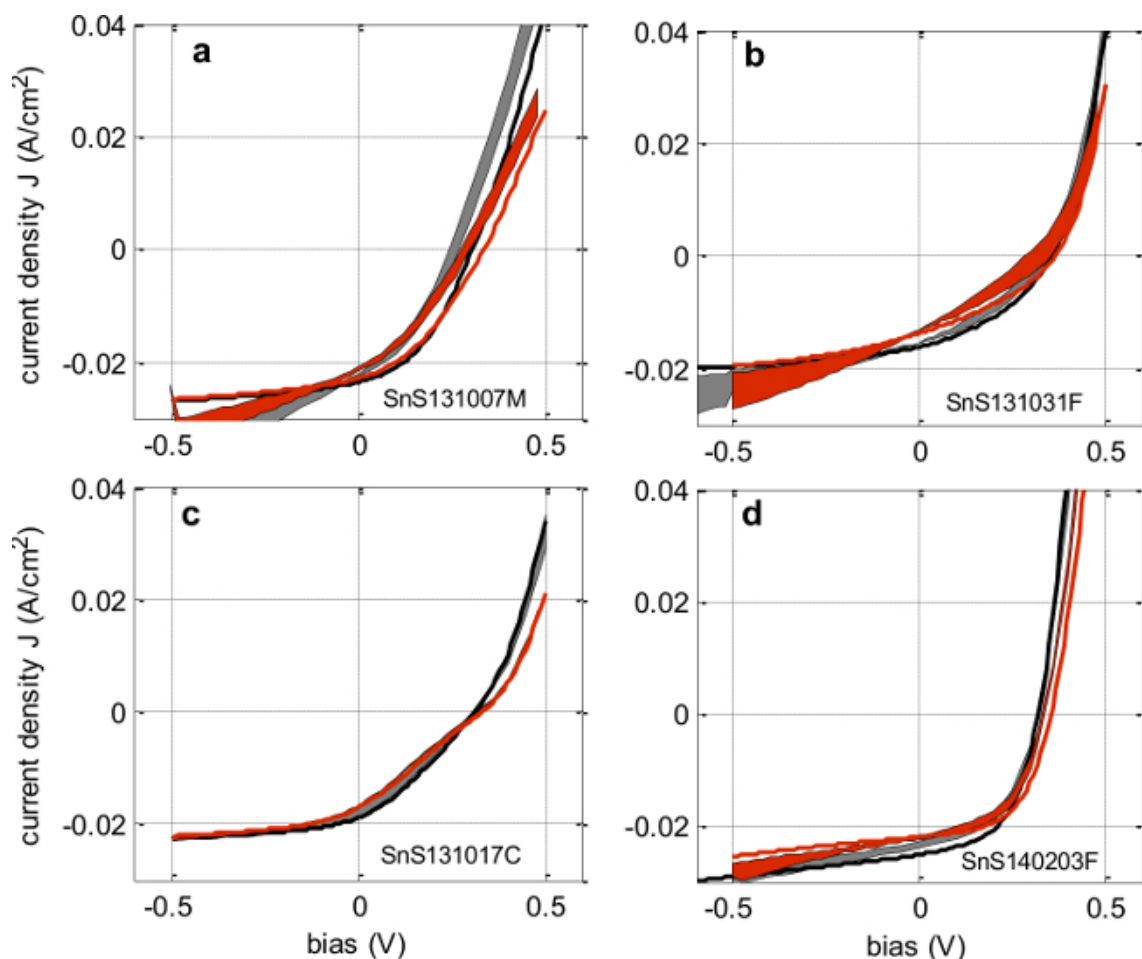


Figure 11. Long-time stability of SnS solar cells. *J-V* tests of samples that were repeatedly measured over a period of nearly a year, while being stored in air and being exposed to ambient light without encapsulation. For each panel the black curves show the initial measurement, the red curves show the final measurement, and dashed curves show. The thin lines show the best device for each test, and the thick curves are representative *J-V* envelopes (average $\pm$ standard error) for all devices on each sample as described in the text. All four panels show TE-grown samples that were processed as described in this manuscript except for the following differences: (a) No H_2S annealing step. (b) Thinner absorber layer, 650 nm thick; no H_2S annealing step; air exposure performed at 200 °C for 30 min. (c) Thinner absorber layer, 650 nm thick; no H_2S annealing step; buffer layer with higher sulfur content and no nitrogen doping. (d) Antireflection coating deposited on top of device stack. The time between measurements was 50 weeks, 48 weeks, 48 weeks, and 28 weeks for panels a, b, c, and d, respectively. [Please click here to view a larger version of this figure.](#)

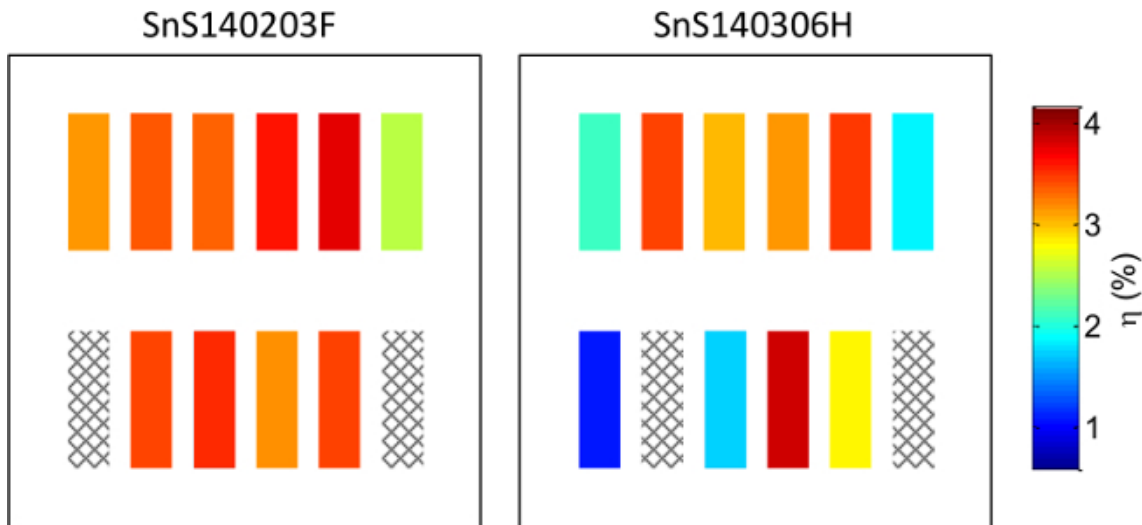


Figure 12. Visualization of spatial non-uniformity across two baseline TE samples. Results are the same as reported in **Figure 6-8**. There are 11 devices on each sample, and each device is color coded according to the measured efficiency; the colormap is the same for both samples. Black-and-white hatching indicates either that the device was not measured, or no device was present (as one corner of each sample).

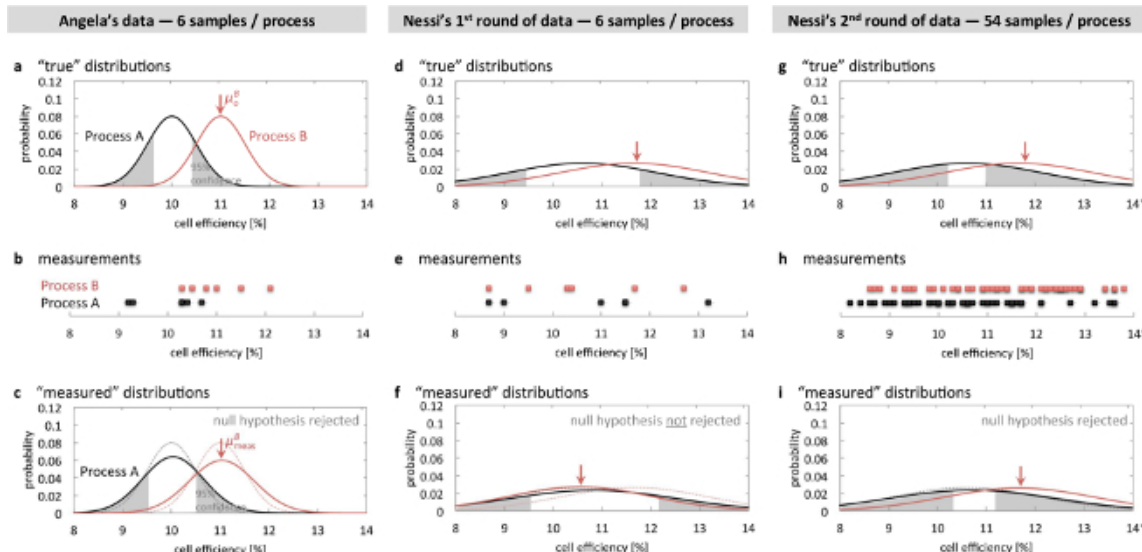


Figure 13. Illustrated example of hypothesis testing in the presence of common cause variance. Fictional characters Angela and Nessi are separately testing the hypothesis that Process B yield higher efficiency solar cells than Process A. Angela has superior process control but a slightly lower baseline efficiency than Nessi. **(A,D,G)** True probability distributions for Angela and Nessi's results. **(B,E,H)** Individual measurements. **(C,F,I)** Measured distributions. With only 6 samples, Angela can reject the null hypothesis but Nessi cannot. See text for full description. [Please click here to view a larger version of the figure.](#)

Discussion

Substrate selection cleaning

Oxidized Si wafers are used as substrates. The substrates are the mechanical support for the resulting solar cells, and their electrical properties are not important. Si wafers are preferred to glass because commercially purchased Si wafers are typically cleaner than commercially purchased glass wafers, and this saves time in substrate cleaning. Si substrates also have higher thermal conductivity than glass, which leads to more even heating during growth and annealing. With commercially purchased glass wafers it was found that it was necessary to clean the substrates with detergent, including a manual rub with gloved fingers followed by a warm ultrasonic bath, in order to remove all visible traces of contamination, and even then substrate cleanliness could not be guaranteed. It was experimentally confirmed that the choice of glass or Si substrates has no impact on device performance. However, this comparison was performed with devices were in the 2% – 3% efficient range, and repeated comparisons will be worthwhile as the baseline efficiency improves.

Typically 10 or more substrates are cleaned at a time using a custom designed quartz wafer carrier. This yields more reproducible results than handling wafers individually with tweezers.

Mo sputtering

It was decided to deposit the Mo back contact (the cathode) in-house rather than purchase Mo-coated substrates after disappointing results were obtained with the substrates available from several different vendors. With purchased substrates (sputtered Mo on glass) problems were encountered with cleanliness, delamination, or both. The Mo film is deposited by DC magnetron sputtering in two layers, one for adhesion to the Si / SiO₂ substrate and one for high conductivity, according to the results published by Scofield *et al.*¹³

Typical Mo films are 720 nm thick with a sheet resistance of approximately 1 Ω/sq. The sheet resistance is measured on a sacrificial substrate using a four point probe system after each Mo growth run. In addition, the adhesion to the substrate is tested using a scalpel blade. Well-adhered films can withstand scratching by hand with a scalpel at moderate pressure without de-laminating. Poorly adhered films will de-laminate with only slight pressure. It was observed that a short substrate plasma cleaning step in the sputtering chamber before Mo growth is important to obtain good adhesion. Typical parameters for this cleaning step are 20 mTorr Ar, 20 W RF, and 60 sec.

SnS growth by thermal evaporation

SnS is evaporated from source powder using a commercially purchased low temperature effusion cell with a pyrolytic boron nitride crucible with volume 32 cm³. When the source is first loaded it is a fine powder and dark grey in color. Typically 3-4 g of powder is loaded. With new source powder, the source temperature is approximately 540 °C in order to maintain a growth rate of 1 Å/sec on a substrate heated to 240 °C. With an increasing number of growth runs, the source temperature must be increased to maintain a constant growth rate. When the required source temperature reaches 610 °C the powder is exchanged.

Closely connected to the source temperature is the issue of SnS flakes. When the growth rate is increased to over 10 Å/sec, large SnS flakes can be observed in the growing film. It is unknown whether these originate from the main source, or from secondary sources such as the effusion cell shroud or the source shutter.

One remarkable observation is that when a batch of source powder is exhausted it leaves behind a white, porous residue at the bottom of the crucible. X-ray diffraction confirms that this is SnO₂. The weight of this residue is typically 0.01 g.

SnS growth by ALD

A critical parameter in this process is the pressure of the nitrogen carrier gas that flows to the Sn(amd)₂ precursor. The pressure is maintained near 250 Torr, but may vary a little bit from time to time. Given that the volume ratio of the Sn(amd)₂ precursor bubbler and N₂ gas trap is 5:1, the pressure inside the bubbler is around 50 Torr. If this value becomes too large, the evaporation of Sn precursor will be significantly suppressed. On the other hand, if the pressure inside the bubbler is too small, there would not be a sufficient pressure drop between the bubbler and the reaction furnace (which has a pressure of ~10 Torr) to enable a smooth gas flow. Either of these scenarios will result to inadequate Sn precursor in the ALD reaction. An indication of this problem is that film thickness near the outlet of the reaction furnace is much thinner than that near the inlet. During each deposition, the pressure inside the reactor is monitored to make sure that the system pressures sit in the correct range.

To ensure a uniform temperature distribution within the reaction zone, the inlet and outlet of the hot-wall deposition tube are wrapped with heating tapes. Under the heating tapes, a pair of thermocouples are inserted to measure the temperature. A non-uniform temperature distribution inside the reaction zone will result to different SnS film morphologies at different regions. At higher deposition temperature, films tend to be rougher and have a lighter color. At low temperatures below 200 °C, films have a higher reflectivity, as can be examined by eye.

SnS annealing in an H₂S tube furnace

The purpose of the annealing step is to optimize the morphology, crystallinity, and electrical properties of the SnS films. For the TE-grown solar cells, the annealing step is performed in a dedicated tube furnace. This 2" diameter quartz tube furnace is capable of flowing mixtures of 4% H₂S (balance N₂), 4% H₂ (balance N₂), pure N₂ and pure Ar. Temperatures are controlled by external Nichrome heating elements and monitored using a quartz-encased thermocouple located in the hot zone. Gas is evacuated using an oil pump filled with inert oil. Seals are made using H₂S resistant elastomers. Typical base pressure is 8-20 mTorr.

The annealing temperature of 400 °C is a balance between secondary grain growth and film re-evaporation. In principle, higher annealing temperature might be beneficial for device performance, and could be achieved without significant film loss by using higher furnace pressure. This is the subject of active investigation.

SnS surface passivation with a native oxide

The purpose of the passivation step is to reduce the density of electronic trap states at junction between the absorber and the buffer layers, and to serve as a diffusion barrier to prevent unwanted mixing of the constituent elements of the absorber and buffer layers.¹⁴ It has been observed that samples processed with this oxidation step have higher V_{OC} values than samples processed without.

At this time, the oxidation step has not been extensively studied and is probably not optimized. Using X-ray photoelectron spectroscopy results (not shown) it is estimated that the oxide should be less than 1 nm thick for good performance and to avoid current blocking.

Deposition of the transparent conducting oxide (TCO), indium tin oxide (ITO)

Prior to this point care is taken to control the total air exposure of the samples at each step. However, after the buffer layer deposition air exposure is no longer limited and the samples are stored and transported in ambient air.

Prior to this point, all depositions have been "blanket" films, covering the entire substrate. From this point on the depositions are patterned to define individual devices. For both the ITO and metallization steps the depositions are defined using laser-cut metal shadow masks. For the ITO deposition it is very important that the area of the deposited pad is sharply defined by the shadow mask. If the area is not sharply defined, for

example due to flexing of the mask in the mask aligner, then the active area of the resulting devices may be significantly larger than the nominal size of 0.25 cm^2 . This can lead to erroneous over-reporting of the current density.

Metallization

The metallization pattern is designed to enable the illumination spot of the quantum efficiency measurement tool to fall completely on the ITO without overlapping with the metal. This constraint results in 2 fingers separated by 1.5 mm, each 7 mm long, and a $1 \times 1 \text{ mm}^2$ contact pad, see **Figure 4**. This pattern is less than optimal from a device-performance standpoint. A pattern optimized for device performance would use more fingers with smaller spacing.

Ag has been used for TE-grown cells and Ni / Al has been used for ALD-grown cells. This division is historical and is not grounded in an experimental outcome. It is possible that Ni / Al provides superior resistance to corrosion during long storage times. In fact, it has been observed that Ag contacts have a tendency to corrode during extended storage in air (for example, longer than a year).

Device characterization

Finished devices are characterized using current-voltage (J - V) measurements collected and external quantum efficiency (EQE) measurements collected with and without white light and voltage bias. To-date solar cells have been measured by contacting individual devices one-at-a-time, using probe micromanipulators in a typical probe station configuration. The solar simulator and EQE systems were physically disconnected, so the sample needed to be re-contacted for each measurement. As a result, it would take approximately 4 – 5 hr to measure J - V and EQE on all 11 devices.

An integrated high-throughput test station that combines J - V and EQE using a single sample chuck and a probing card that contacts all devices simultaneously was recently installed at MIT, see **Figure 5**. The electrical connections are controlled by a programmable multiplexer, and the motorized X-Y chuck stage is computer controlled. In this way, J - V and EQE measurements can be performed sequentially on all 11 devices in under 1 hr.

For routine device testing an area-defining light aperture is not used. Therefore the active device area may be under-estimated, resulting in over-estimates of the current density. However an aperture is used by certification laboratories, often resulting in lower efficiencies (*c.f.* **Figures 7, 9 and 10**). Using an area-defining light aperture is always desirable, but for routine testing it is often neglected due to practical concerns such as to minimize physical contact with the top of the sample. Systematic error due to under-estimating the active device area can be mitigated by using larger device areas. For the work described here, the rather small (0.25 cm^2) size was chosen as appropriate for early stage technology development (at earlier stages an even smaller device of 0.03 cm^2 with no metallization was used). Now that the devices are in the range of 4% efficient and are repeatable, it is worth increasing to a size of 1 cm^2 or more.

In addition to the standard characterization techniques described above, on occasion samples are also tested using techniques including temperature-dependent J - V , Suns- V_{OC} , capacitance-voltage profiling, and lock-in thermography. These techniques are used to understand and quantify specific loss mechanisms such as interface recombination and series resistance loss.

The significance of sharing device fabrication protocols

In publications on inorganic thin film PV the results of device tests are never (with experience) accompanied by sufficient experimental details to reproduce the experiment. This situation leads to unnecessary frustration among individual researchers, and hampers the progress of the whole field. This situation also makes it difficult to compare the procedures described herein to those used by other research groups. The techniques described in this manuscript were developed with the aid of numerous conversations with researchers in thin film PV (mainly in the United States), and a lot of trial-and-error. The authors hope that this work helps others avoid unnecessary frustrations, and sets a precedent for details reporting of experimental methods in thin film PV.

Future applications of the described protocol

The protocol described herein is used to establish a “baseline” SnS solar cell. The most important feature of a baseline fabrication protocol is repeatability; the absolute efficiency number is less important. In the authors’ experience, repeatability is the key attribute that will enable ongoing research to improve efficiency, such as by improving surface passivation or reducing bulk defect density. Without a repeatable baseline protocol it is extremely difficult to judge the effects of changes to the fabrication protocol. This is fully described in the section below on hypothesis testing.

Ongoing and future work on SnS solar cells will leverage the baseline protocol described here to optimize the individual fabrication steps with the goal of increasing device efficiency. Of particular interest are the H_2S annealing and the surface passivation steps, since these directly impact the defect density in the bulk of the absorber and at the p - n junction.

Data ensembles enable hypothesis testing

In a field that idolizes champion efficiencies, it is tempting to overlook the ensemble — the >99% of (non-champion) devices — and the useful information it provides. This section motivates ensemble data analysis, and presents facile approaches for visualizing and extracting useful insights from ensemble data. It is presupposed that the reader has a working understanding of experimental statistics (hypothesis testing), and is comfortable calculating a Gaussian distribution, standard deviation, standard error, and 95% confidence intervals for a given data set.

Simply put, ensemble data analysis is the study of variability, which when reduced, enables better hypothesis testing. Variability, colloquially “noise,” obfuscates the “signal” during hypothesis-driven process engineering and scientific research. As noise increases, more experiments are rendered inconclusive. Inconclusive experiments are a waste of time, resources, and optimism. Ensemble data can help reduce variability in two ways:

First, ensemble data reveal process non-uniformities in space and time. This type of variability is systematic (e.g., caused by temperature- or flow-rate-gradients within a given thin-film deposition chamber), yielding a clear spatially resolved pattern of performance variation, exemplified by **Figure 12**. The spatial or temporal variation embodies the “fingerprint” of the offending process step. *In-situ* metrology and control samples can help identify and troubleshoot sources of systematic process variability.

Second, ensemble data reveal “luck-of-the-draw” or “common-cause” variance, *i.e.*, statistical variability that affects all ensemble elements equally. This variability is more difficult to troubleshoot, because it is the aggregate result of multiple coupled processing steps. Common-cause variance can best be minimized by stringent process controls and standard operating procedures at each step — admittedly a challenging proposition in a fast-changing and minimally staffed academic environment. Nevertheless, the following exercise illustrates why reducing common-cause variance is essential.

The impact of common-cause variance exemplified: A friendly, fictional scientific competition between Dr. Meticulous and Dr. Messy: Angela and Nessi are researchers from two different laboratories. They are engaged in a friendly scientific competition to test the hypothesis that Process B generates better devices than a well-accepted baseline Process A. Both researchers employ a standard hypothesis-testing procedure, which assumes that common-cause variance results in Gaussian efficiency distributions (more representative statistical distribution functions include log-normal for distributions without outliers, and the more statistically robust log-Cauchy-Lorenzian for distributions with strong outliers).

Angela is known to her colleagues as “Dr. Meticulous.” She endeavors to reduce process variability. Angela does not share her beakerware with others, employs chamber pre-conditioning routines before thin-film deposition, incorporates control samples with every fabrication run, and prefers IC-grade silicon substrates with thermal oxide surfaces instead of the more variable glass surfaces. She produces baseline (Process A) devices with a “true” (*i.e.*, actual) mean efficiency of 10% and a true standard deviation (σ_{true}) of 0.5%. Device fabrication and measurements are time consuming, and she is only able to fabricate and measure six devices ($N = 6$) per process.

In another lab, Nessi is hard at work. To her colleagues, Nessi is known as “Dr. Messy.” Her fabrication and metrology tools are located in a shared-use facility. When it’s her turn to use them, she doesn’t take the necessary precautions to ensure low common-cause variance. But because of her sloppiness, her true standard deviation is 1.5% absolute (3× greater than Angela’s). This higher σ_{true} reflects less well-controlled experimental conditions. However, because Nessi uses higher-purity feedstock materials, her baseline Process A achieves a true mean of 10.6%. Nessi fabricates and measures $N = 6$ devices per process.

Let’s suppose that Process B improves “true” device efficiency by 10% relative (*i.e.*, 10% improves to 11%; 10.6% improves to 11.7%). Both Angela and Nessi apply the central limit theorem to the $N = 6$ devices they each fabricate, as shown in **Figure 13**. Note that the “true” distributions (**Figures 13A, D, G**) are hidden to the researchers; they only observe their experimental data (**Figures 13B, E, H**) and the resulting Gaussian fits, standard errors, and confidence intervals (**Figures 13C, F, I**).

On one hand, Angela’s tighter process control (lower variability, smaller σ_{true}) allows her to reject the null hypothesis, concluding with >95% confidence that Process B is superior to Process A (**Figure 13C**). On the other hand, Nessi, who has higher σ_{true} , cannot conclude that Process B is better than Process A (**Figure 13F**) with $N = 6$. Even though Nessi is lucky to make two devices with efficiencies that are higher than any of Angela’s (**Figures 13B, E**), Angela is winning the race to publish the scientific paper that will revolutionize the way her field thinks about Process B.

Nessi realizes that she needs to increase her confidence intervals, which requires her to reduce her standard measurement error (SE), *i.e.*,

$$SE \equiv \frac{\sigma_{\text{measured}}}{\sqrt{N}}. \quad [1]$$

Nessi can pursue one of two approaches to match Angela’s 3× smaller SE: Nessi can reduce her true variability (σ_0) by a factor of 3, or increase N by a factor of $3^2 = 9$. Nessi gains access to a high-throughput device-measurement apparatus, increasing N by 9×. This improvement offsets her 3× greater process variability, and she is able to detect a statistically significant difference between Processes A and B, rejecting the null hypothesis with >95% certainty (**Figure 13I**). She is back in the race for publication.

Higher baseline efficiencies increase the odds of successful hypothesis testing: Focusing on the equation for SE (**Equation 1**), it can be seen how increasing baseline performance increases the odds of successful hypothesis testing. If the aforementioned Process B were tested on a 5%-efficient baseline device instead of 10%, the absolute efficiency improvement would be only 0.5% instead of 1%. Assuming σ_0 is unchanged, the minimum number of samples required to reject the null hypothesis increases by 4×. Thus, improving baseline device performance has the same mathematical effect as reducing σ , *i.e.*, a 1-to-1 improvement in confidence intervals.

Final word: Reducing standard error is essential to minimize the risk of inconclusive hypothesis tests. Standard error can be reduced by decreasing common-cause variance, manifest in σ_0 , which results in a 1-to-1 reduction in SE. Improving baseline performance has an equivalent effect. One can also increase sample size N , but this will have a weaker impact on SE because of the square root (increasing N also increases the risk of systematic variation).

The importance of applying experimental statistics is widely accepted in biology and physics (*c.f.* standing statistics committees at all high energy experiments).¹⁵ To improve the quality of data reporting in PV, it is recommended that researchers pay attention to the 99% of devices they fabricate, and adopt hypothesis testing with data ensembles.

Disclosures

The authors have nothing to disclose.

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References

1. Woodhouse, M., Goodrich, A., *et al.* Perspectives on the pathways for cadmium telluride photovoltaic module manufacturers to address expected increases in the price for tellurium. *Solar Energy Materials and Solar Cells*. **115**, 199-212 (2013).
2. *Bloomberg New Energy Finance University 2013 - renewable energy, CCS, EST*. Available from: <http://about.bnef.com/presentations/bnef-university-renewable-energy-ccs-est/> (2013).
3. Ramakrishna Reddy, K. T., Koteswara Reddy, N., Miles, R. W. Photovoltaic properties of SnS based solar cells. *Solar Energy Materials and Solar Cells*. **90**, (18-19), 3041-3046 (2006).
4. Sinsermsuksakul, P., Heo, J., Noh, W., Hock, A. S., Gordon, R. G. Atomic Layer Deposition of Tin Monosulfide Thin Films. *Advanced Energy Materials*. **1**, (6), 1116-1125 (2011).
5. Noguchi, H., Setiyadi, A., Tanamura, H., Nagatomo, T., Omoto, O. Characterization of vacuum-evaporated tin sulfide film for solar cell materials. *Solar Energy Materials and Solar Cells*. **35**, 325-331 (1994).
6. Hartman, K., Johnson, J. L., *et al.* SnS thin-films by RF sputtering at room temperature. *Thin Solid Films*. **519**, (21), 7421-7424 (2011).
7. Tanusevski, A. Optical and photoelectric properties of SnS thin films prepared by chemical bath deposition. *Semiconductor Science and Technology*. **18**, (6), 501 (2003).
8. Sharma, R. C., Chang, Y. A. The S-Sn (Sulfur-Tin) system. *Bulletin of Alloy Phase Diagrams*. **7**, (3), 269-273 (1986).
9. Steinmann, V., Jaramillo, R., *et al.* 3.88% Efficient Tin Sulfide Solar Cells using Congruent Thermal Evaporation. *Advanced Materials*. **26**, (44), 7488-7492 (2014).
10. Sinsermsuksakul, P., Sun, L., *et al.* Overcoming Efficiency Limitations of SnS-Based Solar Cells. *Advanced Energy Materials*. **4**, (15), 1400496 (2014).
11. Hejin Park, H., Heasley, R., Gordon, R. G. Atomic layer deposition of Zn(O,S) thin films with tunable electrical properties by oxygen annealing. *Applied Physics Letters*. **102**, (13), 132110 (2013).
12. Palmeshofer, L. Rutherford Backscattering Spectroscopy (RBS). *Surface and Thin Film Analysis*. 191-202 Available from: <http://onlinelibrary.wiley.com/doi/10.1002/9783527636921.ch11/summary> (2011).
13. Scofield, J. H., Duda, A., Albin, D., Ballard, B. L., Predecki, P. K. Sputtered molybdenum bilayer back contact for copper indium diselenide-based polycrystalline thin-film solar cells. *Thin Solid Films*. **260**, (1), 26-31 (1995).
14. Malone, B. D., Gali, A., Kaxiras, E. First principles study of point defects in SnS. *Physical Chemistry Chemical Physics*. **16**, 26176-26183 (2014).
15. Vaux, D. L. Research methods: Know when your numbers are significant. *Nature*. **492**, (7428), 180-181 (2012).