Video Article

Fabrication of Uniform Nanoscale Cavities via Silicon Direct Wafer Bonding

Stephen R. D. Thomson[1], Justin K. Perron[2,3], Mark O. Kimball[4], Sarabjit Mehta[5], Francis M. Gasparini[1]

[1]Department of Physics, The State University of New York at Buffalo

[2]Joint Quantum Institute, University of Maryland

[3]The National Institute of Standards and Technology

[4]Cryogenics and Fluids Branch, NASA Goddard Space Flight Center

[5]HRL Laboratories

Correspondence to: Francis M. Gasparini at fmg@buffalo.edu

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Abstract

Measurements of the heat capacity and superfluid fraction of confined ^{4}He have been performed near the lambda transition using lithographically patterned and bonded silicon wafers. Unlike confinements in porous materials often used for these types of experiments[3], bonded wafers provide predesigned uniform spaces for confinement. The geometry of each cell is well known, which removes a large source of ambiguity in the interpretation of data.

Exceptionally flat, 5 cm diameter, 375 μm thick Si wafers with about 1 μm variation over the entire wafer can be obtained commercially (from Semiconductor Processing Company, for example). Thermal oxide is grown on the wafers to define the confinement dimension in the z-direction. A pattern is then etched in the oxide using lithographic techniques so as to create a desired enclosure upon bonding. A hole is drilled in one of the wafers (the top) to allow for the introduction of the liquid to be measured. The wafers are cleaned[2] in RCA solutions and then put in a microclean chamber where they are rinsed with deionized water[4]. The wafers are bonded at RT and then annealed at ~1,100 °C. This forms a strong and permanent bond. This process can be used to make uniform enclosures for measuring thermal and hydrodynamic properties of confined liquids from the nanometer to the micrometer scale.

Video Link

The video component of this article can be found at http://www.jove.com/video/51179/

Introduction

When clean silicon wafers are brought into intimate contact at RT, they are attracted to each other via van der Waals forces and form weak local bonds. This bonding can be made much stronger by annealing at higher temperatures[5,6]. Bonding can be done successfully with surfaces of either SiO_2 to Si or SiO_2 to SiO_2. Bonding of Si wafers are most commonly used for silicon on insulator devices, silicon-based sensors and actuators, and optical devices[7]. The work described here takes wafer direct bonding in a different direction by using it to achieve well-defined uniformly-spaced enclosures over the entire wafer area[8,9]. Having a well-defined geometry where fluid can be introduced allows measurements to be performed in order to determine the effect of the confinement on the properties of the fluid. Hydrodynamic flows can be studied where the small dimension can be controlled from tens of nanometers to several micrometers.

SiO_2 can be grown on Si wafers using a wet or dry thermal oxide process in a furnace. The SiO_2 can then be patterned and etched as desired using lithographic techniques. Patterns which have been used in our work include a pattern of widely spaced support posts which results upon bonding in a planar or film geometry (see **Figure 1**). We have also patterned channels for one-dimensional characteristics, and arrays of boxes, either of $(1\ \mu m)^3$ or $(2\ \mu m)^3$ dimension[1] (see **Figure 2**). When designing a confinement with boxes, typically 10-60 million on a wafer, there needs to be a way to fill all of the individual boxes. A separate patterning of the top wafer with a design that stands off the two wafers by 30 nm or more allows for this. Or, equivalently, shallow channels can be designed on the top wafer so that all the boxes are linked. The thickness of the oxide grown on the top wafer is different from that on the bottom wafer. This adds another degree of flexibility and complexity to the design. Being able to pattern both wafers allows for a larger variety of confinement geometries to be realized.

The size of the geometric features in these bonded wafers, or cells, can vary. Cells with planar films as small as 30 nm have been made successfully[10,11]. At thicknesses below this, overbonding can take place whereby the wafers bend around the support posts thus "sealing" the cell. Recently, a series of measurements on liquid ^{4}He have been performed with an array of $(2\ \mu m)^3$ boxes with varying separation distance between them[10,12]. Features much larger in depth than 2 μm are not very practical due to the increasing length of time required to grow the oxide. However, measurements have been made with an oxide as thick as 3.9 μm[9]. The limits on the smallness of the lateral dimension arise from the limits of the lithography capabilities. The limit for the largeness of the lateral dimension is determined by the size of the wafer. We have successfully created planar cells where the lateral dimension spanned almost the entire wafer diameter, but one could just as easily imagine

patterning several smaller structures on the order of tens of nanometers in width. However such structures would require e-beam lithography. We have not done this at this time.

In all of our work the bonded wafers formed a vacuum tight enclosure. This is achieved by retaining in the patterned oxide a solid ring of SiO_2 of 3-4 mm in width at the perimeter of the wafer, see **Figure 1**. This, upon bonding, forms a tight seal. This design could be easily modified if one were interested in hydrodynamic studies which require an input and an output.

The bursting pressure of the bonded cells has also been tested. We found that with 375 μm thick wafers, pressure up to approximately nine atmospheres could be applied. However, we have not studied how this could be improved by bonding over larger oxide areas or, perhaps, for thicker wafers.

The procedure for interfacing the silicon cells to a filling line and the techniques for measuring the properties of the confined helium at low temperature is given in Mehta *et al.*[2] and Gasparini *et al.*[13] We note that changes in linear dimension for silicon are only 0.02% upon cooling the cells[14]. This is negligible for the patterns formed at RT.

Protocol

1. Before Bonding, Wafer Preparation

This step except for 1.8 is done in the Cornell Nanoscale Facility cleanroom.

1. Grow the oxides in a standard thermal oxidation furnace using a wet oxide process for thick oxides and, to achieve better thickness control, a dry oxide process for very thin oxides. Check the thickness for uniformity over the full wafer with ellipsometry.
2. Create a mask for the geometry you wish to etch.
3. Spin photoresist on the wafers being etched.
4. Expose, develop and bake a test wafer and examine with an appropriate microscope.
5. If the test wafer is exposed as desired, etch the test wafer. The ratio of oxide thickness to lateral feature dimension will determine if a wet or dry etch is appropriate. Since the wet etches are isotropic they will not produce vertical walls in the oxide. In many cases this does not matter. If vertical walls are desired one can use reaction ion etching. If the etching is successful, proceed with the other wafers. Often, the hydrophobic/hydrophilic properties of Si and SiO_2 can be used to see if the etching process has been successful.
6. Remove the photoresist from the wafers. For most photoresists, this can be done initially with isopropyl alcohol and acetone. However, some small amount of resist will still remain on the wafers. This resist needs to be completely removed in order to achieve good bonding.
7. Use a brief 20 min oxygen descumming process in a reactive ion etcher. This will remove whatever photoresist remains on the wafers. However, this will also add some oxide layers to the exposed silicon. This is typically 1-4 nm[15].
8. Drill the filling hole in the top wafer. This can be done with diamond tipped drill bits and smart-cut lubrication (see Materials for manufacturer details). Rinse off the smart-cut immediately after drilling with deionized water. Drilling can also be done using a diamond paste with 3-9 μm grit for filling holes larger than ~0.124 cm in diameter. Smart-cut can again be used for lubrication. We use a small precision drill press at 1,000-2,000 rpm.

2. Bonding Preparation

1. In order to bond wafers, cleanliness is paramount. There are a few steps that should be taken to clean the wafers. First, clean with RCA baths.
    1. Rinse wafers in deionized (DI) water.
    2. Clean in "RCA" acid bath. RCA acid bath is H_2O:H_2O_2:HCl with the ratios of 5:1:1. Place wafers in 80 °C RCA acid for 15 min with the patterned sides facing up. This step will eliminate any metallic contamination.
    3. Remove wafers from the acid and rinse in DI water bath for 5 min.
    4. Clean in the "RCA" base next. RCA base is H_2O:H_2O_2:NH_4OH with the ratios of 10:2:1. Place wafers in 80 °C RCA base for 15 min with the patterned sides facing up. This step will eliminate any organic contamination.
    5. Rinse wafers in DI water bath for ~15 min.
2. The wafers need to be removed from the DI water bath and remain clean in order for proper bonding to occur. This is done in two steps:
    1. First, place the wafers with their patterned etched sides facing each other on a Teflon chuck in a clean microchamber as shown in **Figure 3B**. They are separated by ~1 mm Teflon tabs. Spray deionized water between the wafers while they spin slowly (~10-60 rpm) for ~2 min in order to remove any particle contamination. A film of water will be left between the wafers at this point. This prevents dust contamination prior to the next step.
    2. Cover the wafers with the clear acrylic lid and spin the wafers dry for ~30 min at 3,000 rpm. Use a 250 W infrared heat lamp to aid the drying process. The rapid spinning will entrain any particle contaminants with the ejection of the water film, as in **Figure 3C**.
3. Before removing the lid over the wafers, remove the tabs separating the wafers by rotating the lid. This will bring the wafers into light local contact while still in the microclean chamber. Now the wafers may be safely removed from the microclean chamber on their carrier. The very small gap of approximately 1 μm between the wafers will minimize dust contamination during this step. Also, do not pick up the wafers with tweezers at this point since this would initiate asymmetric bonding. Instead, transport the wafers with the use of the removable carrier onto the arbor press.

3. Wafer Bonding

1. Press the two wafers together using an arbor press and a fairly rigid and smooth (Nerf) ball. The Nerf ball is used to apply pressure to the wafers from the middle outward. Pressure applied this way allows trapped air to be pushed out as the bonding wave spreads from the center out. Starting the bonding at the center minimizes the stresses which are built up as the wafers contour to each other. The wafers have a free-state flatness of about 1 µm, while the gaps achieved in the bonding are uniform within a few nm. Thus, the wafers must distort from their free state in order to achieve this.
    1. Check the bonding by looking for interference fringes using an infrared light source and detector with a 1 µm high pass filter. Sample images are shown in **Figures 4** and **5**. Interference fringes (Newton rings) will appear if there is poor bonding. If bonding is good, one can proceed to step 3.3. If bonding is poor and there are nonuniformities, proceed as follows.
    2. Place the cell on an optical flat, cover with filter paper to protect and cushion the top wafer, and press the wafers together with wafer tongs. Push debonded "bubbles" to either the middle (where there is the filling hole) or to the edges. Be careful when applying force near the edges since the wafers may be slightly offset center to center. Pressure near the edges therefore may cause the top wafer to crack if it overhangs the bottom wafer.
    3. If the bonding irregularities persist or a dust particle is evident, split the wafers by wedging a razor blade between them. Repeat the process from the beginning (step 2.1.1). Up to this point, the bonding is reversible. The wafers can be rebonded at RT many times while trying to get acceptable bonding.

2. After obtaining acceptable RT bonding, one proceeds to anneal the wafers. Temperatures above 900 °C need to be reached in order to be certain of proper annealing[5,6].
    1. Stage the cell onto a quartz vacuum chuck such that the filling hole is centered over the pumping hole in the chuck. The chuck is connected to a quartz pumping tube which is used to evacuate the cell prior and during the annealing process. This tube extends outside the furnace. Evacuating the cell causes a pressure of one atmosphere to be applied to the cell. This will help with the bonding. Pumping is also necessary to prevent pressure build up if the furnace temperature is ramped up too quickly. The time it takes to significantly lower the pressure in the cell will depend on the geometry within the cell.
    2. To avoid the growth of oxide on the outside of the cell, purge the furnace chamber with a nonreacting gas, typically ^{4}He, so that no oxide is grown.
    3. To allow for strains to have time to relax, it is important to ramp temperatures from 250-1,200 °C over the course of ~4 hr. After staying at 1,200 °C for at least 4 hr, turn off the furnace.
    4. Allow the system to cool to RT.

3. Analyze the cell once again using the infrared light source and detector as shown in **Figure 6**. If annealing went well, the cell will look as good as, or often better than, when initially put in the furnace. If there are unacceptable fringes indicating poor bonding, the entire process must be repeated from the beginning; however, this must be done with new wafers. Once annealed, the bond between wafers is permanent and there is no splitting possible.

Representative Results

Properly bonded wafers will have no unbonded regions. Attempting to split the wafers after annealing will cause the cell to break into pieces due to the strength of the bond. Infrared images of properly bonded wafer are shown in **Figures 5** and **6**. Often annealing improves the uniformity of the cell, especially if local unbonded regions are due to lack of flatness in the wafers. In **Figure 5** the light spots and border are bonded areas. The center bright spot is the hole for filling the cell. In the dark areas the wafer are at a 0.321 µm separation. The only unbonded region in **Figure 5** is near the border on the top left side of the image. Since it is located beyond the edge of the oxide border, and thus could not be filled with liquid, this would not affect the use of this cell.

There are multiple symptoms of poor bonding which can manifest, however the most common is having a trapped particle between the wafers. This will cause localized lack of bonding to occur and is visible via the appearance of interference Newton rings in the infrared image, as in **Figure 4A**. This cell has a broad oxide ring on the outside and within this region we can see several small rings indicating unbonded regions. Also, near the center, where a square pattern of channels are formed (not visible), there is a pattern of several Newton rings. These cells would not be suitable for use. In **Figure 4B** we have attempted to close the unbonded region by applying pressure locally. This is partly effective, and there are fewer rings, but still there remain small inhomogeneities. These wafers were then split and the bonding process was restarted.

Another possible poor-bonding scenario is overbonding. This occurs when there are not enough support posts between the wafers to maintain uniform separation, or the posts are not large enough, thus causing the cell to collapse,[16] *i.e.* bonding directly silicon to silicon. Bowing of the wafers occurs between posts to the point where there is no longer any gap between the wafers. This is not easily observed via the infrared imaging and is generally only discovered when the cell is unable to be filled. Overbonding is a significant concern mainly when dealing with very small gaps (tens of nanometers) where the van der Waals forces are greatest.

A third potential problem with bonding wafers is that sometimes wafers, no matter how clean, simply are not flat enough to bond. Although rare, because of the exceptionally flat wafers used, sometimes poor bonding between wafers will persist. The bonding process involves two wafers overcoming their free-state flatness and contouring to each other at a uniform separation. This necessitates a substantial stress on both wafers and may lead to lack of bonding because of excess stress. The thicker the wafer, the more difficult bonding is since the wafers lose flexibility[6]. When persistent lack of bonding occurs, one should use a new wafer and attempt bonding again. If bonding again is poor in the same general locations of the wafer, the reused wafer is not flat enough for bonding and must be replaced.

To achieve uniform cell structures the wafers are studied at RT both before and after bonding. Before bonding, the thickness of the oxide grown on the silicon before patterning is measured using ellipsometry. After patterning, an atomic force microscope can be used to confirm dimensions. More complicated or smaller patterns require using an electron microscope to analyze the pattern. After bonding the wafers at a desired separation, Fabry-Perot interferometry can be used to determine the local separation of the bonded structure. With multiple measurements

along the face of the bonded wafers, the separation between them can be mapped as shown in **Figure 7**. The Fabry-Perot method uses the interference of transmitted light as it is multiply reflected by the parallel surfaces in the cell. However, this can only be used if the spacing is greater than half the cutoff absorption wavelength for Si. Thus, the lower limit for verifying bonding with Fabry-Perot interferometry is about 0.57 μm[9]. These methods, combined with the infrared imaging of the cell, confirm the uniformity of the cell structure.

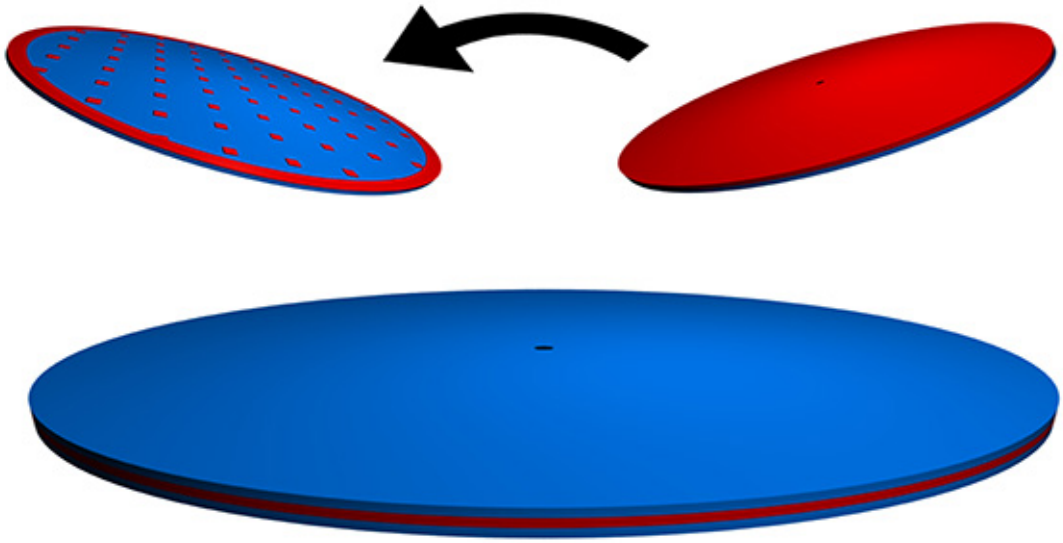

Figure 1. Schematic drawing of two wafers ready to be bonded together (upper). The blue represents the Si while red represents SiO_2. The left wafer has been patterned lithographically with support posts. The right wafer has not been patterned in this example, although often it will be patterned. Combining the two wafers as indicated creates a planar geometry of uniform separation interrupted by the support posts. The wafers are bonded together at RT (lower). This bond is weak, and the wafers will need to be annealed to strengthen the bond. Click here to view larger image.

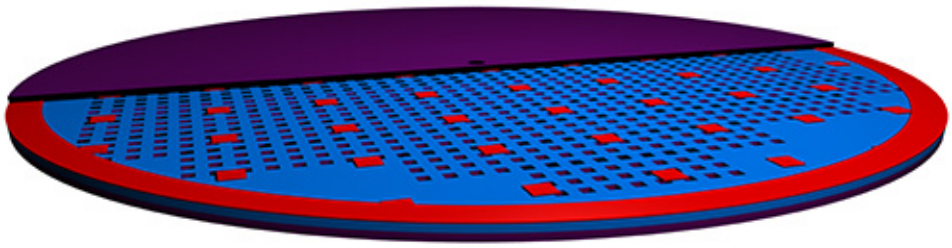

Figure 2. A cross-sectional drawing of two patterned wafers bonded together. The bottom wafer has boxes which have been etched in the oxide using ion beam lithography (these are the dark purple squares). The top wafer has support posts, shown by the red squares, which keep the top waver 33 nm above the bottom wafer. These features are not to scale in this drawing. Click here to view larger image.

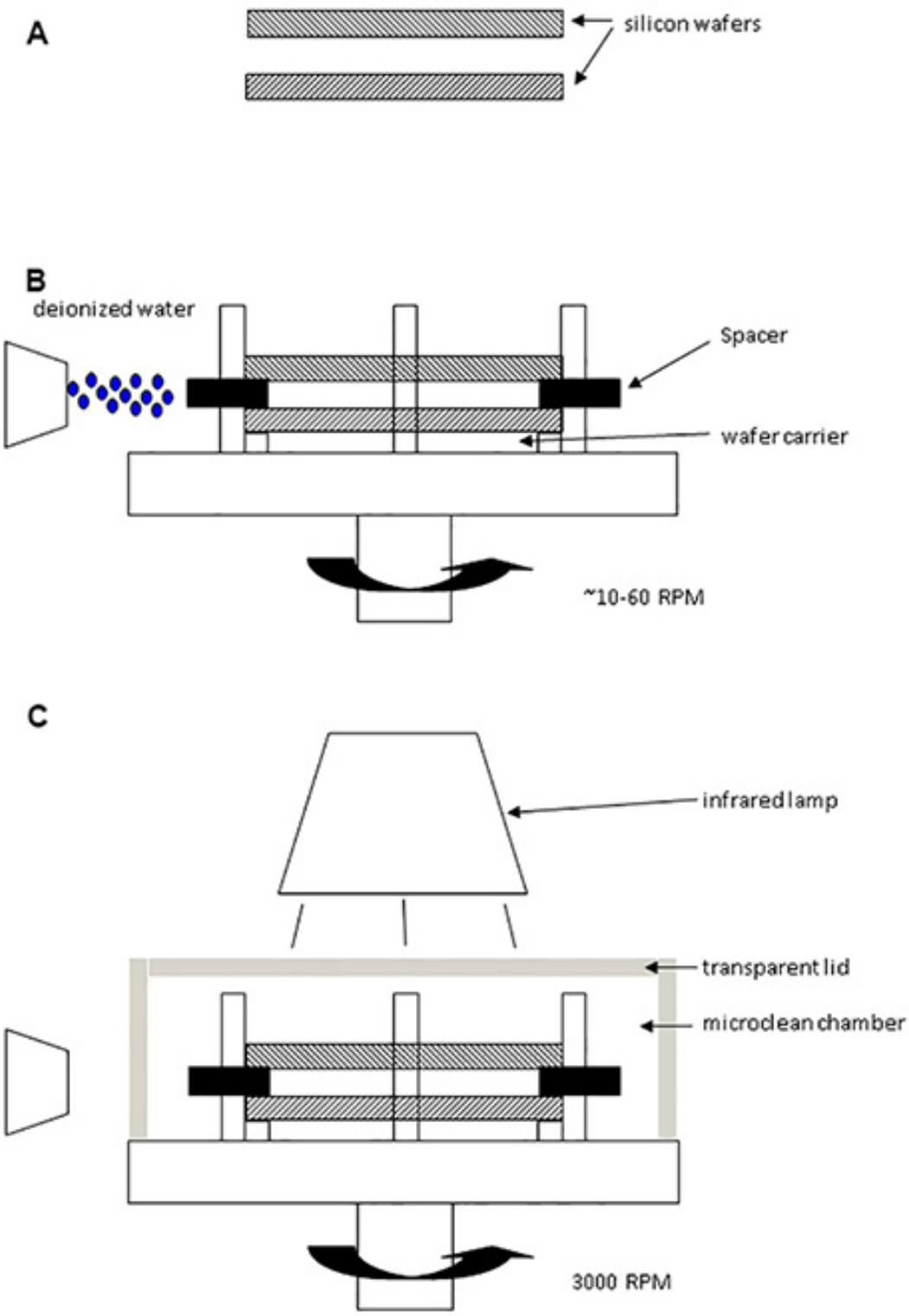

Figure 3. Schematic diagram of the RT rinsing and drying process in the micro-clean chamber. A) shows the two wafers. **B**) the wafers have been placed on the spinner and are separated a distance of approximately 1 mm by three spacer tabs. A jet of deionized water is sprayed between the wafers as they spin slowly. **C**) the wafers have been covered and are spun at 3,000 rpm to dry them under an infrared heat lamp. After this process, the separating tabs are moved out of the way by rotating the cover before exposure to the laboratory environment. Click here to view larger image.

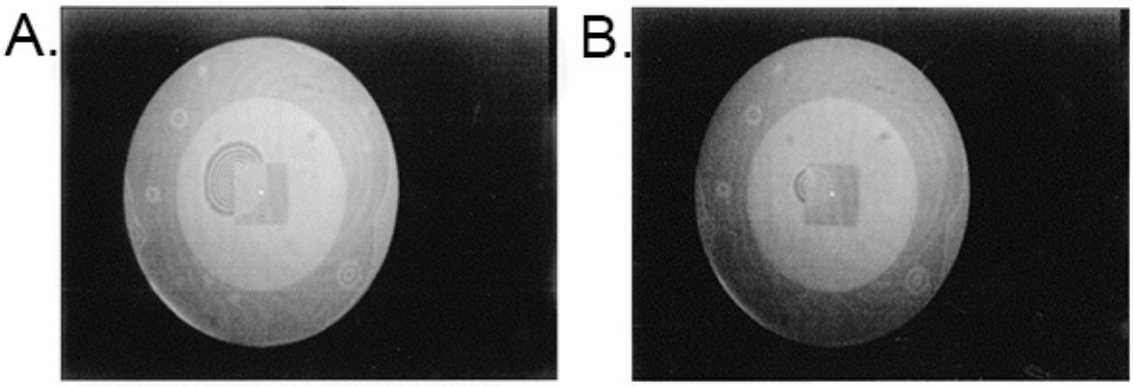

Figure 4. A) Infrared images of a cell after initial RT bonding. There are some clearly unbonded areas (light rings) in the border which are not large enough to compromise the use of the cell. However, near the center the multiple rings indicate that there is an unbonded area where the separation is ~3 µm. **B**) After attempting to force bonding in this region by applying a pressure locally, it is clear that there is a particle trapped between the wafers near the center causing the lack of bonding. These wafers will have to be split and the process restarted. Note that throughout the images there is a faint waviness seen most clearly along the bonded dark broad border. This is due to the variations of thickness of the silicon wafers themselves and not their separation. Click here to view larger image.

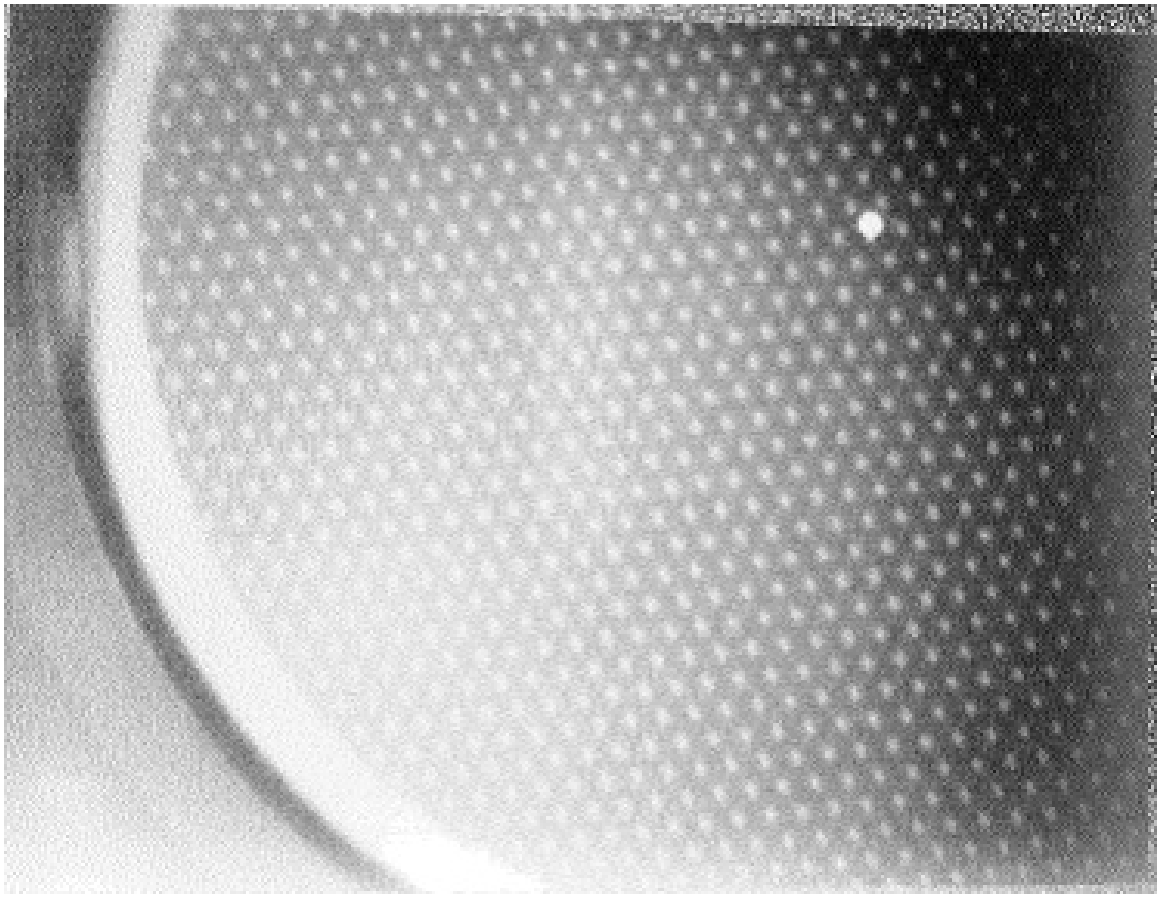

Figure 5. A close up infrared image of a section of a cell. Because of the thickness of the oxide grown for this cell, 0.321 µm, the support posts can clearly be seen in this image as the regular light spots throughout the cell. The bright spot in the center is the filling hole. A slight lack of bonding can be seen at the edges of the image on the left side. Click here to view larger image.

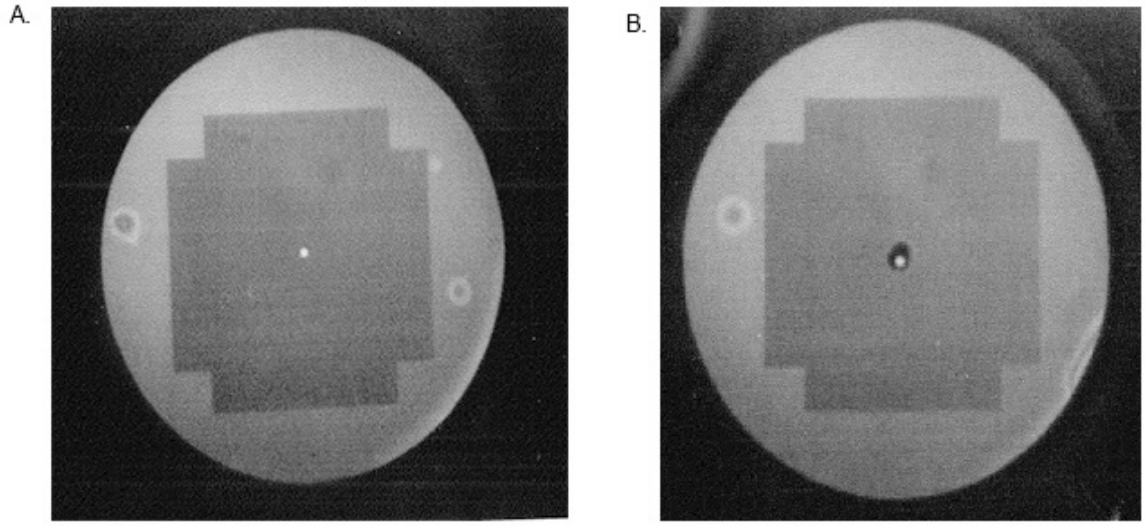

Figure 6. Infrared image of a cell immediately before (A) and after (B) annealing. There are two places where there is a lack of bonding, as evidenced by the light rings. Annealing caused the location and size of the unbonded areas to change. The "squarish" patter covering most of the wafer is the active area for experimental use. This is completely uniform. The dark area around the bright center hole is likely a chemical reaction due to backstreaming from the mechanical pump. Click here to view larger image.

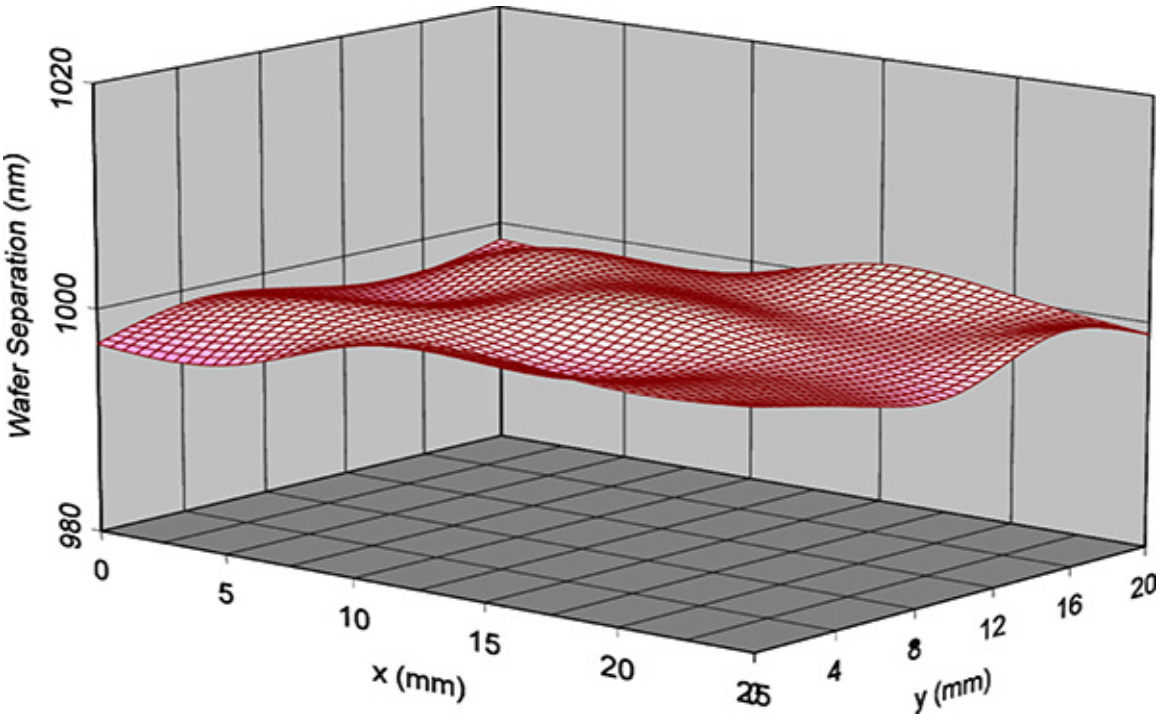

Figure 7. Typical uniformity of spacing for well bonded wafers. This plot was obtained using Fabry-Perot interferometry in a series of measurements over an area ~20 mm x 20 mm on the bonded wafers. The cell was designed for a separation of 0.989 µm. As measured, the bonded wafer agrees well with this to better than one percent. Click here to view larger image.

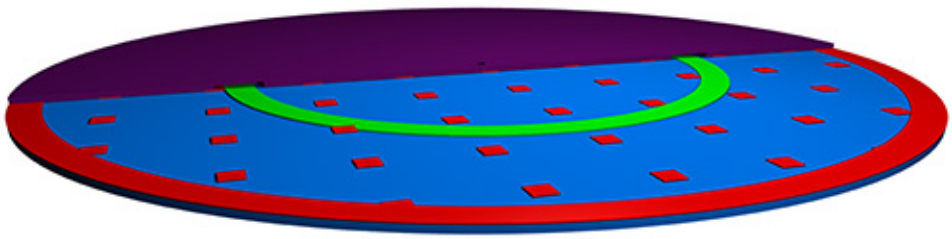

Figure 8. A cross-sectional drawing of wafers patterned with a Corbino[17] ring geometry. Two regions are isolated from each other by a ring. A thin film of 30 nm will be formed on top of this ring by the pattern on the top wafer. The resulting geometry will have two relatively large chambers separated by a nanofilm. Click here to view larger image.

Discussion

The development of suitable silicon lithography in combination with direct wafer bonding has allowed us to make vacuum tight enclosures with highly uniform small dimensions over all the full area of a 5 cm diameter silicon wafer. These enclosures have allowed us to study the behavior of liquid ^{4}He in the neighborhood of its phase transitions from a normal liquid to a superfluid. These studies have verified predictions of finite-size scaling, as well as pointed out failures which remain to be explored. The work has also identified, for the first time, a very strong coupling that exists between two regions of liquid when separated by a very thin, ~30 nm film. Studies along these lines are continuing with cells designed in the Corbino geometry, as shown in **Figure 8**. This geometry has two region isolated from each other by a ring and connected only by a film 30 nm thick.

Our method of cell construction is limited because SiO_2 thickness much greater than 2 μm is difficult to achieve. This is because of the long furnace growth time. In the other limit, large planar structures with separation smaller than ~30 nm are difficult to achieve while avoiding overbonding. Overbonding happens when the two wafers bend over the support posts and touch. One way to avoid this is to use thicker wafers and/or space the support posts closer together. We have not explored all of these variables fully. A thicker wafer in particular might prevent overbonding, however it may also be too stiff and not bond to give a uniform separation. We have achieved separation as small as 10 nm in a structure where studies were made in channel of widths ranging from 2-20 μm[18]. In this limit one has to worry about the short range variations in the surface of the silicon which can be mapped out with an Atomic Force Microscope[18].

There are other bonding methods which can be considered. Electrostatic bonding can be used for glass bonding to silicon. This process is more suitable for bonding over a small area since one initiates bonding with an electrode at high voltage and the bonding wave starts wherever the surfaces are closest together. Thus the bonding wave is not symmetric over the surface of the wafers. Another bonding technique with which we experimented had a similar problem. In our earlier bonding procedures we initiated bonding by using tweezers to pick up the wafers from the microclean chamber. This was not satisfactory. Thus, as described, we went to the use of a holder and the initiation of bonding using a ball press. This step could also be improved since we have not explored the parameters for optimum ball stiffness and press arrangement.

Overall successful bonding of silicon must start with exceptionally flat wafers. Ours are specified to be flat with 1 μm over the full 5 cm size. Since we have spaced two wafers as close as 30 nm, one can see that there must be substantial deformation of the wafers as they bend to achieve this separation. This suggests that wafers cannot be too thick. We have not explored variations in wafer thickness since we have been successful with 375 μm.

Small cavities can also be achieved using a process of anodic bonding, using either glass on glass[19] or glass on silicon[20]. These techniques have yielded planar cavities in the 30 nm to 11 μm range. These structures have a smaller cross section than the cells we make by more than an order of magnitude, 0.2-0.7 cm^2 vs 12 cm^2 for our cells. They can also be made without support posts because much thicker glass and silicon are used. Thus, while their techniques represent another viable way of achieving micro- to nanofluidic chambers, it would seem to us that direct wafer bonding with the possibility of patterning both wafers is a more variable technique which has allowed the formation of two dimensional, one dimensional, and zero dimensional structures. The cells from Dimov *et al.*[19] and Duh *et al.*[20] would not be suitable for our own measurements.

Disclosures

We have nothing to disclose.

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References

1. Gasparini, F. M., Kimball, M. O., Mooney, K. P. & Diaz-Avila, M. Finite-size scaling of He-4 at the superfluid transition. *Rev. Mod. Phys.* **80**, 1009-1059, doi:10.1103/RevModPhys.80.1009 (2008).
2. Mehta, S., Kimball, M. O. & Gasparini, F. M. Superfluid transition of He-4 for two-dimensional crossover, heat capacity, and finite-size scaling. *J. Low Temp. Phys.* **114**, 467-521, doi:10.1023/A:1021858305720 (1999).
3. Reppy, J. D. Superfluid-Helium in Porous-Media. *J. Low Temp. Phys.* **87**, 205-245, doi:10.1007/Bf00114905 (1992).
4. Mehta, S. *et al.* Silicon wafers at sub-mu m separation for confined He-4 experiments. *Czech. J. Phys.* **46**, 133-134 (1996).
5. Tong, Q. Y., Cha, G. H., Gafiteanu, R. & Gosele, U. Low-Temperature Wafer Direct Bonding. *J. Microelectromech. S.* **3**, 29-35 (1994).
6. Tong, Q. Y. & Gosele, U. Semiconductor Wafer Bonding - Recent Developments. *Mater. Chem. Phys.* **37**, 101-127, doi:10.1016/0254-0584(94)90080-9 (1994).
7. Gosele, U. & Tong, Q. Y. Semiconductor wafer bonding. *Annu. Rev. Mater. Sci.* **28**, 215-241, doi:10.1146/annurev.matsci.28.1.215 (1998).
8. Rhee, I., Petrou, A., Bishop, D. J. & Gasparini, F. M. Bonding Si-Wafers at Uniform Separation. *Physica B.* **165**, 123-124, doi:10.1016/0921-4526(90)90453-2 (1990).
9. Rhee, I., Gasparini, F. M., Petrou, A. & Bishop, D. J. Si Wafers Uniformly Spaced - Bonding and Diagnostics. *Rev. Sci. Instrum.* **61**, 1528-1536, doi:10.1063/1.1141166 (1990).
10. Perron, J. K., Kimball, M. O., Mooney, K. P. & Gasparini, F. M. Critical behavior of coupled ^{4}He regions near the superfluid transition. *Phys. Rev. B.* **87**, 094507 (2013).
11. Perron, J. & Gasparini, F. Specific Heat and Superfluid Density of ^{4}He near T λ of a 33.6 nm Film Formed Between Si Wafers. *J. Low Temp. Phys.* 1-10, doi:10.1007/s10909-012-0795-0 (2012).
12. Perron, J. K. & Gasparini, F. M. Critical Point Coupling and Proximity Effects in He-4 at the Superfluid Transition. *Phys. Rev. Lett.* **109**, doi:Artn 035302Doi 10.1103/Physrevlett.109.035302 (2012).
13. Gasparini, F. M., Kimball, M. O. & Mehta, S. Adiabatic fountain resonance for He-4 and He-3-He-4 mixtures. *J. Low Temp. Phys.* **125**, 215-238, doi:10.1023/A:1012967823431 (2001).
14. Corruccini, R. J. & Gniewek, J. J. *Thermal expansion of technical solids at low temperatures; a compilation from the literature*. U.S. Dept. of Commerce, National Bureau of Standards (1961).
15. Kahn, H., Deeb, C., Chasiotis, I. & Heuer, A. H. Anodic oxidation during MEMS processing of silicon and polysilicon: Native oxides can be thicker than you think. *J. Microelectromech. S.* **14**, 914-923, doi:10.1109/Jmems.2005.851802 (2005).
16. Tong, Q. Y. & Gosele, U. Thickness Considerations in Direct Silicon-Wafer Bonding. *J. Electrochem. Soc.* **142**, 3975-3979, doi:10.1149/1.2048444 (1995).
17. Corbino, O. M. Azioni Elettromagnetiche Doyute Agli Ioni dei Metalli Deviati Dalla Traiettoria Normale per Effetto di un Campo. *Nuovo Cim.* **1**, 397-420, doi:10.1007/BF02958241 (1911).
18. Diaz-Avila, M., Kimball, M. O. & Gasparini, F. M. Behavior of He-4 near T-lambda in films of infinite and finite lateral extent. *J. Low Temp. Phys.* **134**, 613-618, doi:10.1023/B:Jolt.0000012617.06353.17 (2004).
19. Dimov, S. *et al.* Anodically bonded submicron microfluidic chambers. *Rev. Sci. Instrum.* **81**, doi:Artn 013907 Doi 10.1063/1.3291107 (2010).
20. Duh, A. *et al.* Microfluidic and Nanofluidic Cavities for Quantum Fluids Experiments. *J. Low Temp. Phys.* **168**, 31-39, doi:10.1007/s10909-012-0617-4 (2012).

