Video Article

# Monolayer Contact Doping of Silicon Surfaces and Nanowires Using Organophosphorus Compounds

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## Abstract

Monolayer Contact Doping (MLCD) is a simple method for doping of surfaces and nanostructures[1]. MLCD results in the formation of highly controlled, ultra shallow and sharp doping profiles at the nanometer scale. In MLCD process the dopant source is a monolayer containing dopant atoms.

In this article a detailed procedure for surface doping of silicon substrate as well as silicon nanowires is demonstrated. Phosphorus dopant source was formed using tetraethyl methylenediphosphonate monolayer on a silicon substrate. This monolayer containing substrate was brought to contact with a pristine intrinsic silicon target substrate and annealed while in contact. Sheet resistance of the target substrate was measured using 4 point probe. Intrinsic silicon nanowires were synthesized by chemical vapor deposition (CVD) process using a vapor-liquid-solid (VLS) mechanism; gold nanoparticles were used as catalyst for nanowire growth. The nanowires were suspended in ethanol by mild sonication. This suspension was used to dropcast the nanowires on silicon substrate with a silicon nitride dielectric top layer. These nanowires were doped with phosphorus in similar manner as used for the intrinsic silicon wafer. Standard photolithography process was used to fabricate metal electrodes for the formation of nanowire based field effect transistor (NW-FET). The electrical properties of a representative nanowire device were measured by a semiconductor device analyzer and a probe station.

## Video Link

The video component of this article can be found at http://www.jove.com/video/50770/

## Introduction

Controlled surface doping of semiconductor structures with macroscopic areas as well as at the nanoscale is important for advanced semiconductor device architectures such as FinFet[2,3], as well as for nanostructure based devices such as nanowire-based sensors and photovoltaics[4-7]. We recently introduced monolayer contact doping (MLCD) for repeatable, uniform surface doping of silicon interfaces with macroscopic and nanometric dimensions with control over dopant dose and diffusion profile[1]. An important feature of MLCD is the restriction of monolayer formation to a substrate that is termed "donor substrate". MLCD simplifies some of the process steps required for Monolayer Contact Doping (MLCD) and provides complementary surface doping capabilities[8]. Once the donor substrate is loaded with the dopant containing monolayer by using self-limiting surface chemistry, the donor substrate is brought to contact with the substrate intended for doping, termed "target substrate", and both substrates are annealed while in contact. During the anneal process, dopant atoms diffuse to both donor and target substrates, and are activated at the elevated temperature. Since MLCD does not require high energy implantation of dopant atoms, no structural damage is caused to the semiconductor lattice during the process and no further anneal step is required. Good control over dopant diffusion is possible by controlling the rapid thermal process parameters. Ultra shallow and uniform dopant diffusion lengths down to a few nanometers are easily achieved. Separation of the monolayer from the process sequence simplifies the process, allow greater control over process parameters and open new possibilities for doping schemes that were not possible by using other methods. Achieving dopant level as high as the solubility limit of phosphorus in silicon is possible by multiple MLCD doping processes applied successively. In summary, traditional doping methods suffer from intrinsic limitations to fabricate ultra-shallow doping profiles. This is because of inherent statistical variations of source concentrations, overall dose and energy distribution, which are inherent to the low implantation energies required for ultra-shallow implantation. MLCD provides a simple means for surface doping, this is the result of the unique features of MLCD relying on the precise control of dopant dose and location at the atomic scale by utilizing robust surface chemistry for generating the dopant source with self-limiting monolayer chemistry formed exclusively at the semiconductor surface.

 

## Protocol

# 1. Surface Cleaning

1. Prepare acidic piranha solution by mixing 1:3 hydrogen peroxide (30%) and concentrated sulfuric acid.

   Caution: Piranha solutions are extremely strong and dangerous oxidizing agents and should be used with extreme caution. These solutions may explode in contact with organic solvents. Only qualified personnel with appropriate training and safety equipment may perform the procedure.
2. Place substrates (later used as donor and target substrates) in appropriate holder and insert into piranha solution for 15 min.
3. Rinse samples in DI water 3x.
4. Prepare base piranha solution by mixing 1:1:5 ammonium hydroxide (25%), hydrogen peroxide (30%) and DI water.
5. Place substrates (later used as donor and target substrates) in appropriate holder and insert into the base piranha solution and place in ultrasonic bath at 60 °C for 8 min.
6. Rinse samples in DI water 3x.
7. Rinse samples in ethanol then blow dry under a stream of nitrogen.
8. Dry samples in an oven at 115 °C for 10 min.

# 2. Monolayer Formation

1. Prepare a 1% v/v solution of tetraethyl methylenediphosphonate in mesitylene.
2. Place donor substrates in a pressure-safe vial containing the methylenediphosphonate mesitylene solution, seal, and heat at 100 °C for 2 hr.

   Important: Heating the solvent in a sealed vial generates pressure. Caution must be taken that the vessel used is appropriate and will withstand the generated pressure. The closed vial with solvent should not be heated close to or above the solvent boiling point. The vial may not be opened while hot.
3. Let the vial cool down, open the vial, and rinse samples 3x in mesitylene, 3x in dichloromethane and blow dry under nitrogen stream.

   * For doping of nanowires continue to step 3, for doping of wafers move to step 5.

# 3. Nanowire Synthesis

1. Clean a microscope glass slide in oxygen plasma for 2 min.
2. Apply a few drops of poly-L-lysine solution on the slide to fully cover it, wait for 5 min then rinse with DI water and blow dry with nitrogen.
3. Apply a few drops of gold colloid solution on the slide to fully cover it, wait 2 min then rinse with DI water and blow dry with nitrogen.
4. Remove organic contaminants by using oxygen plasma for 30 sec.
5. Insert the glass slide with gold nanoparticles to a CVD chamber and evacuate.
6. Pre equilibrate the chamber at 440 °C, 35 torr and 50 sccm flow of $H_2$.
7. Start the deposition process by flowing $SiH_4$ gas, 2 sccm flow. Perform the CVD process for 30 min in order to obtain nanowires of roughly 50 µm length.
8. Measure the length of nanowires (by SEM or by optical microscope using a dark field filter). If using an optical microscope measure the length of nanowires standing at the sample edges, there it should be easy to find a wire sticking out parallel to the surface.

# 4. Nanowire Drop-casting onto Substrate

1. Suspend the nanowires in ethanol. Place the slide with nanowire film prepared in step 3 in a vial and add ethanol to cover the slide with excess liquid level of ~1 cm.
2. Sonicate the vial for 3 sec, the solution should become slightly turbid.

   Important: The suspended nanowires tend to aggregate since the suspension is not stable; therefore it should be used shortly after preparation, prior to aggregation taking place.
3. Place $Si_3N_4/SiO_2/Si$ substrate on a hot plate pre heated to 150 °C. Add few drops of nanowire suspension onto the heated surface. Once the liquid is dried, check the density of nanowires on the surface following the drop cast process using an optical microscope with dark field filter. In order to achieve high yield of single nanowire devices the process should result with surface density of about 100 nanowires per 1 $mm^2$ with minimal nanowire length of ~20 µm.

# 5. Rapid Thermal Anneal

1. Place the target substrate (intrinsic Si wafer or nanowires drop casted into a substrate from previous steps) on the donor substrate such that the target is facing towards the donor substrate.
2. Place the two substrates in the RTA chamber and close the chamber door.
3. Evacuate the chamber, purge with Argon, then evacuate again. This step ensures that no oxygen or other undesired gas residues are left in the chamber.
4. Anneal the substrates at desired temperature and time. The doping level, indicated by sheet resistance value, depends on anneal time and temperature (**Figure 1**). A process of 1,000 ºC anneal temperature and 40 sec anneal time is demonstrated. Typically, anneal times of 5-120

sec are applied. The temperature ramp time should be as short as possible, depending on the anneal system specifications. Here, a 6 sec ramp time is used from room temperature to the process temperature.

## 6. Sheet Resistance Measurements

1. Dip the MLCD doped sample in 1% hydrofluoric acid solution for 5 min for removal of the oxide layer.
2. Rinse with DI water, isopropanol and blow dry with nitrogen stream.
3. Measure sheet resistance using a four point probe setup. For this example, the Jandel RM3-AR is used and has a dedicated automatic sheet resistance measurement system. Typical current applied is in the range of 1-10 µA.

## 7. Nanowire Device Fabrication and Characterization

1. Heat the sample on a hot plate at 120 °C for 5 min.
2. Spin coat AZ nLOF2020 photoresist at 4,000 rpm.
3. Bake the sample at 110 °C for 75 sec using vacuum hot plate.
4. Expose at 40 mJ/cm$^2$ with 365 nm light source using a mask aligner and the electrodes pattern mask.
5. Bake the samples again after exposure at 110 °C for 75 sec on a vacuum hot plate.
6. Develop the samples in AZ726MIF solution for 70 sec, rinse in DI water and blow dry with nitrogen stream.
7. Evaporate 100 nm of Nickel by e-beam evaporator.
8. Perform lift-off by hot (80 °C) N-Methyl-2-pyrrolidone (NMP) solvent.
9. Inspect the substrate to locate NW-FET devices successfully formed in the process and register their locations. This can be done easily using optical microscope with dark field filter provided that address markers are formed.
10. Measure I-V curves for selected devices by using a semiconductor device analyzer and probe station setup. Place the sample on the conductive stage which is connected to the analyzer as the gate terminal. Use the microscope camera of the probe station to approach the probe needles near the device electrodes and gently touch the electrodes with the needles. The needles should be connected as source and drain terminals to the analyzer.

## Representative Results

Representative results for phosphorous-MLCD surface doping process are shown in **Figure 1**. Intrinsic silicon wafers were treated with phosphorous-MLCD, resulting in monotonic decrease in the sheet resistance values. Sheet resistance values decrease for longer anneal times and higher anneal temperatures as shown by the three traces in **Figure 1**. Sheet resistance values can be correlated to activated dopant concentration. Lower sheet resistance values indicate higher doping levels and vice versa. Higher anneal temperature and longer anneal time results in higher doping levels and lower sheet resistance values. Note that further increase in the anneal time will not result in further decrease of sheet resistance since the monolayer dopant source is a limited source, leading to limited source diffusion regime. In fact, for long anneal times often an increase in sheet resistance is observed due to dilution of the dopant by deep diffusion into the intrinsic silicon bulk material.

Typical NW-FET device I-V measurements for intrinsic NW and MLCD-doped devices are presented in **Figure 2**. The *i*-SiNW device exhibits a non-active source drain channel prior to phosphorous-MLCD. Following contact doping, the NW device show increase in conductivity compared to the intrinsic device as demonstrated by the I-V curves with saturation current values >1 µA for gate voltage of 5 V and source-drain bias of 3 V for a moderately doped SiNW. Similarly to doping of bulk surfaces, higher anneal temperatures results in higher doping levels and higher currents through the NW channel. For a highly doped SiNW current values of >50 µA were measured at 5 V gate voltage and 3 V source-drain voltage. Further analysis of the I-V curve may be carried out to calculate $I_{on}/I_{off}$ ratios, charge carrier type and mobility values.

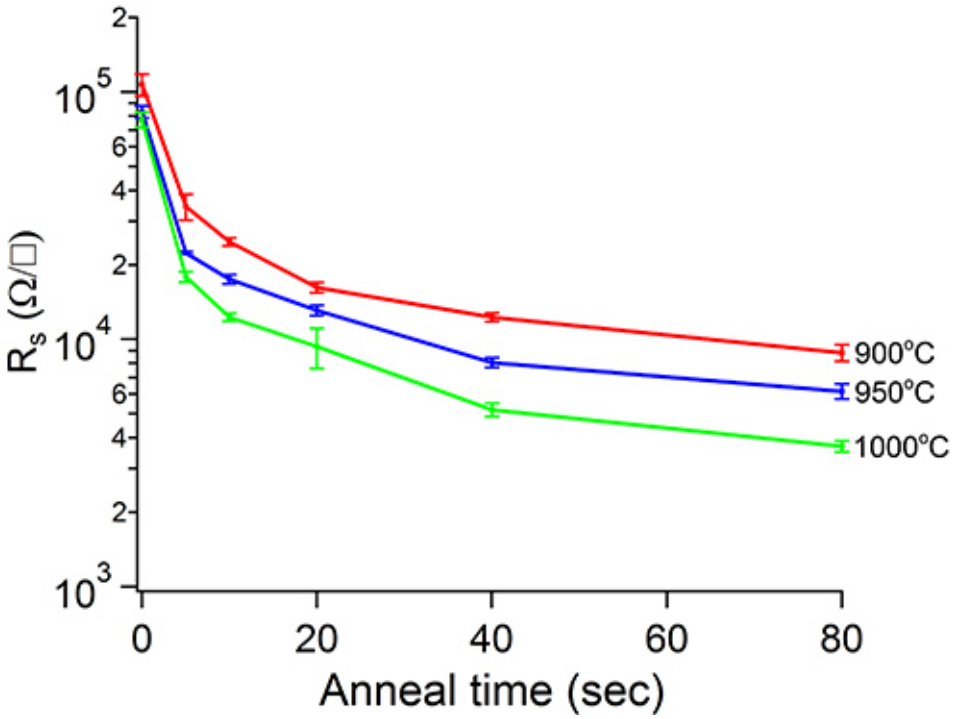


**Figure 1. Sheet resistance ($R_s$) values for target substrate annealed at 900 °C, 950 °C and 1,000 °C for various anneal times.**

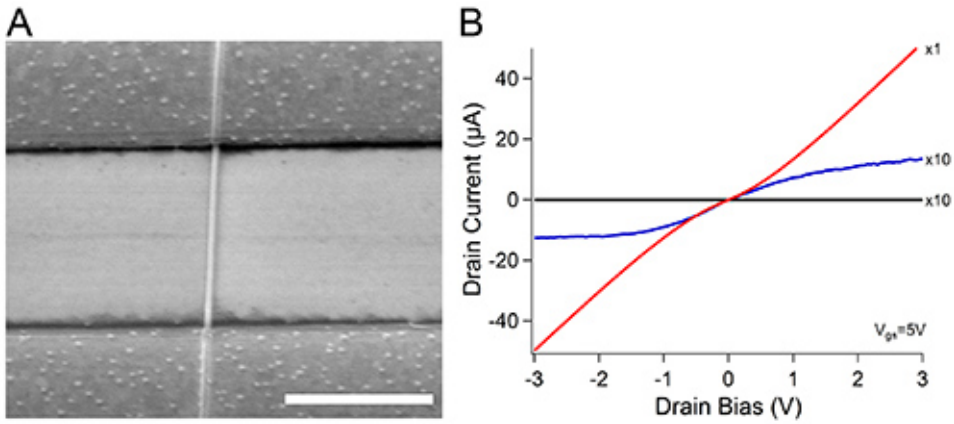


**Figure 2. SEM image showing the NW channel and Source-Drain nickel electrodes scale bar 2 μm (A).** (**B**) I-V curves of intrinsic NW-FET (black) compared to MLCD moderately doped NW-FET (blue) annealed at 900 °C for 30 sec, and highly doped NW-FET annealed at 1,005 °C for 10 sec (red).

## Discussion

MLCD is a simple and reproducible method. However, attention to surface cleaning and monolayer formation must be taken. Piranha cleaning of the surfaces prior to the MLCD process is important not only for the purpose of avoiding possible impurities, but also for initialization of the surface for reproducible monolayer formation providing reproducible results between processes. The piranha treatment results in hydroxylation of surface groups which is required for binding of precursor molecules to the surface for the formation of the monolayer. Cleaning and activation can also be achieved by oxygen plasma although it is not recommended due to incorporation of charged species at the surface which affects the doping results. The resulting doping profiles can be controlled by the anneal time and temperature.

MLCD rely on self-limiting surface chemistry resulting in the formation of single molecular layer (monolayer) of dopant containing molecules at the interface of the donor substrate. Use of a monolayer as the dopant source ensures a well-defined initial dopant dose and dopant is placed at the interface brought to contact with the intended interface for surface doping. MLCD is designed such that the monolayer formation step on the donor substrate is separated from the target substrate. Using a separate substrate for the monolayer formation simplifies the overall surface doping process, does not require the deposition and removal of $SiO_2$ capping layer, allowing removal of the native oxide layer from the target

substrate for enhanced dopant incorporation. Furthermore, intrinsic nanowires doped by MLCD process were shown to exhibit highly uniform longitudinal dopant distribution that is difficult to achieve by in-situ CVD nanowires synthesis[1,9].

Various phosphine oxide precursor molecules may be used as source for monolayer formation. Dopant surface dose can be tuned by the molecular footprint of the precursor, with bulky molecular precursors leading to lower surface density of dopant source. Another way to control the initial dopant surface density is by the formation of mixed monolayers with one component in the mixture having dopant atom and the other component absent. The molecular mixture ratio and surface affinity result in tunable dopant surface concentration. Different precursors exhibit different decomposition mechanisms and therefore results in different doping levels[1].

Further characterization of surfaces doped with MLCD includes TOF-SIMS measurements of dopant diffusion profiles. Doping of nanowires is characterized by fabrication of nanowire based field effect transistors (NW-FET) and electrical measurements of the devices. Nanowires are synthesized using CVD by the vapor-liquid-solid (VLS) mechanism described elsewhere[10,11]. The devices are fabricated by photolithography based on statistical method, without the use of e-beam lithography which is common for this task. The electrodes pattern consist of periodic groups of four metal pads, each group is numbered for identification. The gap between the pads defines the nanowire device channel length and usually designed for ~2 µm. An optical microscope with a dark field filter is used for locating successfully formed devices present between two metal pads and connected by a single nanowire. The I-V characteristics of these devices are measured by a semiconductor analyzer. Annealing of the metal contacts using forming gas is recommended in order to eliminate contact problems and variations. For nickel contacts anneal the sample at 400 °C for 30 sec under forming gas (5% $H_2$, 95% $N_2$).

## Disclosures

No conflicts of interest declared.

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## References

1. Hazut, O., Agarwala, A., *et. al.* Contact doping of silicon wafers and nanostructures with phosphine oxide monolayers. *ACS Nano.* **6** (11), 10311-10318 (2012).
2. Hisamoto. D., Lee, W-C.,FinFET- A self-aligned double-gate MOSFET scalable to 20 nm. *IEEE Trans. Electron Devices*. **47**, 2320-2325 (2000).
3. Leung, G., Chui, C. O., Variability impact of random dopant fluctuation on nanoscale junctionless FinFETs. *IEEE Electron Device Lett.* **33**, 767-769 (2012).
4. Ho, J. C., Yerushalmi, R., *et. al.* Wafer-scale, sub-5 nm junction formation by monolayer doping and conventional spike annealing. *Nano Lett.* **9** (2), 725-730 (2009).
5. Peercy, P. S., The Drive to Miniaturization. *Nature.* **406**, 1023-1026 (2000).
6. Lu, W., Lieber, C. M., Semiconductor Nanowires. *J. Phys. D.* **39**, R387-R406 (2006).
7. Gunawan, O., Wang, K., Fallahazad, B., Zhang, Y., Tutuc, E., Guha, S., High Performance Wire-Array Silicon Solar Cells. *Prog. Photovoltaics.* **19**, 307-312 (2011).
8. Ho, J. C., Yerushalmi, R., Jacobson, Z. A.; Fan, Z.; Alley, R. L.; Javey, A. Controlled nanoscale doping of semiconductors via molecular monolayers. *Nat. Mater.* **7**, 62-67 (2008).
9. Koren, E., Rosenwaks, Y., Allen, J. E., Hemesath, E. R., Lauhon, L. J., Nonuniform. Doping distribution along silicon nanowires measured by kelvin probe force microscopy and scanning photocurrent microscopy. *Appl. Phys. Lett.* **95**, 092105 (2009).
10. Wagner, R. S., Ellis. W. C., The vapor-liquid-solid mechanism of crystal growth and its application to silicon. *Trans. Metall. Soc. AIME.* **233**, 1053-1064 (1965).
11. Cui, Y., Lauhon, L. J., Gudiksen, M. S., Wang, J., Lieber, C. M., Diameter-controlled synthesis of single-crystal silicon nanowires. *Appl. Phys. Lett.* **78**(15), 2214-2216 (2001).

 