Video Article

Nanofabrication of Gate-defined GaAs/AlGaAs Lateral Quantum Dots

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Abstract

A quantum computer is a computer composed of quantum bits (qubits) that takes advantage of quantum effects, such as superposition of states and entanglement, to solve certain problems exponentially faster than with the best known algorithms on a classical computer. Gate-defined lateral quantum dots on GaAs/AlGaAs are one of many avenues explored for the implementation of a qubit. When properly fabricated, such a device is able to trap a small number of electrons in a certain region of space. The spin states of these electrons can then be used to implement the logical 0 and 1 of the quantum bit. Given the nanometer scale of these quantum dots, cleanroom facilities offering specialized equipment- such as scanning electron microscopes and e-beam evaporators- are required for their fabrication. Great care must be taken throughout the fabrication process to maintain cleanliness of the sample surface and to avoid damaging the fragile gates of the structure. This paper presents the detailed fabrication protocol of gate-defined lateral quantum dots from the wafer to a working device. Characterization methods and representative results are also briefly discussed. Although this paper concentrates on double quantum dots, the fabrication process remains the same for single or triple dots or even arrays of quantum dots. Moreover, the protocol can be adapted to fabricate lateral quantum dots on other substrates, such as Si/SiGe.

Video Link

The video component of this article can be found at https://www.jove.com/video/50581/

Introduction

Quantum information science has drawn a lot of attention ever since it was shown that quantum algorithms can be used to solve certain problems exponentially faster than with the best known classical algorithms[1]. An obvious candidate for a quantum bit (qubit) is the spin of single electron confined in a quantum dot since it is a two-level system. Numerous architectures have been suggested for the implementation of quantum dots, including semiconducting nanowires[2], carbon nanotubes[3], self-assembled quantum dots[4], and semiconductor vertical[5] and lateral quantum dots[6]. Gate-defined lateral quantum dots in GaAs/AlGaAs heterostructures have been very successful because of their versatility and their fabrication process is the focus of this paper.

In lateral quantum dots, the confinement of electrons in the direction perpendicular to the sample surface (z direction) is achieved by choosing the proper substrate. The GaAs/AlGaAs modulation-doped heterostructure presents a two-dimensional electron gas (2DEG) confined to the interface between the AlGaAs and the GaAs layers. These samples are grown by molecular beam epitaxy to obtain a low impurity density which, combined with the modulation-doping technique, leads to high electron mobility in the 2DEG. A schematic of the different layers of the heterostructure as well as its band structure are shown in **Figure 1**. A high electron mobility is needed in the 2DEG to ensure the coherence of electronic states over the entire surface of the quantum dot. The substrate used for the fabrication process described below was purchased from the National Research Council of Canada and presents an electron density of $2.2 \times 10^{11} \text{cm}^{-2}$ and an electron mobility of $1.69 \times 10^{6} \text{ cm}^2/\text{Vsec}$.

The confinement of electrons in the directions parallel to the sample surface is achieved by placing metallic electrodes on the surface of the substrate. When these electrodes are deposited on the surface of the GaAs sample, Schottky barriers are formed[7]. Negative voltages applied to such electrodes lead to local barriers in the 2DEG below which only electrons with sufficient energy can cross. Depletion of the 2DEG occurs when the voltage applied is negative enough that no electrons have enough energy to cross the barrier. Therefore, by carefully choosing the geometry of the electrodes, it is possible to trap a small number of electrons between depleted regions of the sample. Control of the number of electrons on the dot as well as the tunneling energy between the dot and the 2DEG in the rest of the sample can be achieved by fine-tuning the voltages on the electrodes. A schematic of the gate electrodes and the depleted electron gas is shown in **Figure 2**. The design for the gate structures forming the dot is inspired by the design used by Barthel *et al.*[8]

To control and read out information regarding the number of electrons on the dot, it is useful to induce and measure current through the dot. Readout can also be done by using a Quantum Point Contact (QPC), which also requires a current through the 2DEG. The contact between the 2DEG and voltage sources is ensured by ohmic contacts. These are metallic pads that are diffused from the surface of the sample all the way down to the 2DEG using a standard rapid thermal anneal process[7] (see **Figures 3a** and **4b**). To avoid short circuits between the source and

the drain, the surface of the sample is etched so that the 2DEG is depleted in certain regions and the current is forced to travel through certain specific channels (see **Figures 3b** and **4a**). The region where the 2DEG still remains is referred to as the "mesa".

The following protocol details the entire fabrication process of a gate-defined lateral quantum dot on a GaAs/AlGaAs substrate. The process is scalable since it remains the same regardless if the device being fabricated is a single, double, or triple quantum dot or even an array of quantum dots. Manipulation, measurement, and results for double quantum dots fabricated using this method are discussed in further sections.

Protocol

The fabrication process described below is done on a GaAs/AlGaAs substrate with dimensions of 1.04 x 1.04 cm. Twenty identical devices are fabricated on a substrate of this size. All steps of the process are done in a cleanroom and appropriate protective gear must be used at all times. Deionized water is used throughout the process, but is simply referred to as "water" in the protocol below.

1. Etching of the Mesa

The result of this fabrication step is shown in Figure 4a.

1. Place the sample in a plasma asher with an O_2 plasma at 75 W for 2 min to remove any traces of undesired resist or organic compounds.
2. Clean the sample in a sonic bath with acetone (2x) and IPA for 5 min each. Blow-dry with a compressed N_2 gun. Throughout the fabrication protocol, when using a sonic bath, avoid using high powers to prevent damaging the GaAs wafer that has a tendency to cleave.
3. Bake the sample in an oven at 125 °C for at least 15 min to dehydrate the surface. Dehydration can also be achieved by placing the sample on a hot plate at 180 °C for at least 5 min.
4. Spin coat the sample with Shipley S1818 photoresist at 3,500 rpm for 30 sec and bake on a hot plate at 115 °C for 60 sec. The resulting layer of resist should be about 2.5 μm thick. S1818 is used because it is thick and is affected very little by the solution used in step 1.11 to etch the substrate. Throughout the fabrication process, it is important to avoid overbaking photoresist and e-beam resist to ensure easy removal in subsequent steps.
5. Use a photolithographic mask aligner and an edge bead mask to expose the resist on the outer edge of the sample. The edge bead mask consists of a 1 x 1 cm chrome square on a glass plate. Use light with a wavelength of 436 nm and expose the resist for 10 sec at 15m W/cm². The wavelength and power are fixed and may vary with the machine used. Adjust the exposure and development times to obtain well-defined features of the proper size.
6. Develop exposed resist by immersing the sample in MF-319 for 2 min 10 sec. Agitate slowly during this step. Rinse in water for 15 sec and blow dry with a compressed N_2 gun. The edge bead should be removed at the end of this step, leaving a 1 x 1 cm surface with a uniform thickness of resist in the middle of the sample. The edge bead is removed before exposing the mesa mask to obtain a better contact between the mask and the sample, which leads to better results.
7. Still using the photolithographic mask aligner, expose the resist using the mesa mask and 436 nm light for 7 sec at 15 mW/cm².
8. Develop the exposed resist by immersing the sample in MF-319 for 2 min 10 sec and agitating slowly. Rinse for 15 sec in water and blow dry with a compressed N_2 gun. The resist remaining on the sample now has the shape of the mesa. The resist will protect this region of the sample from being etched away in the steps that follow.
9. To remove all traces of resist in the previously exposed area, the sample is placed in a plasma asher and is exposed to an O_2 plasma for 1 min at 75 W.
10. A solution of H_2SO_4:H_2O_2:H_2O (5:1:55) is used to etch the sample. Combine the proper proportions of H_2O_2 and water and then add the H_2SO_4. This solution is very reactive when it is first prepared. Wait 20 min before proceeding to the following step to avoid overetching.
11. Etch the sample by immersing it in the acid solution for several seconds and immediately rinsing in water for 30 sec to stop the reaction. The surface of the sample should be etched past the layer of Si dopants and almost all the way down to the 2DEG to ensure depletion in these regions (see **Figure 1**). The etch depth can vary depending on the substrate. Generally, for the type of substrate used, a 34 sec immersion leads to the desired etch depth of 90-100 nm. However, it is important not to overetch to avoid damaging the 2DEG. Since the etch rate varies strongly with the ratio of H_2SO_4 and H_2O_2 in the solution as well as with the wait time before the etch, it is recommended to perform the etching by several immersions of 5-10 sec, instead of a single 34 sec etch, and measure the etched depth with a profilometer after each etch. The relatively slow etch rate of this solution allows for a good control of the etch depth. Cooling the etching solution below room temperature can lead to lower etch rates. However, since it is a shallow etch and the etch profile is unimportant, different etching solutions can also be used.
12. Strip the resist by immersing the sample in 1165 Remover at 65 °C for 3 hr. Rinse in acetone and IPA for 5 min each. Measure the etch profile with a profilometer.

2. Fabrication of the Ohmic Contacts

The result of this fabrication step is shown in Figure 4b.

1. Clean the sample in a sonic bath by immersion in acetone (2x) and IPA for 5 min each. Blow dry with a compressed N_2 gun.
2. Bake the sample in an oven at 125 °C for 15 min to dehydrate the surface.
3. Spin coat with LOR5A at 2,500 rpm for 30 sec and bake on a hot plate at 150 °C for 10 min. Then, spin coat with S1813 at 5,000 rpm for 30 sec and bake on a hot plate at 110 °C for 60 sec. The resulting thicknesses of resist are ~600 nm and ~1.3 μm, respectively. Two layers of resist are used to facilitate the lift-off of the metal that will be deposited in step 2.10.
4. Using a photolithographic mask aligner and the edge bead mask, expose the resist on the outer edge of the sample with 436 nm light for 10 sec at 15 mW/cm².
5. Develop the exposed resist by immersing the sample in MF-319 for 2 min 10 sec while agitating smoothly. Rinse in water for 15 sec and blow dry with a compressed N_2 gun.

6. Still using the photolithographic mask aligner, but this time with the ohmic contact mask, align the patterns for the ohmic contacts on the etched mesa. Expose with 436 nm light for 6 sec at 15 mW/cm^2.

7. Develop the resist in MF-319 for 2 min 10 sec while agitating smoothly. Rinse in water for 15 sec and blow dry with a compressed N_2 gun. There is no longer resist in the regions where the ohmic contacts will be deposited. The developer dissolves the LOR 5A faster than the S1813, leaving an undercut below the top layer of resist. This profile in the resist prevents the metal (that will be deposited in step 2.10) from forming walls at the edges of the resist and will also allow an easy removal of the remaining resist and undesirable metal.

8. To remove all traces of resist in the previously exposed area, place the sample in a plasma asher and expose it to an O_2 plasma for 1 min at 75 W. It is important not to let the sample sit for too long in the plasma because about 75 nm/min of resist is etched during this step.

9. Remove the GaAs native oxide by immersing the sample in a solution of H_2SO_4:H_2O (1:5) for 30 sec and rinsing in water for 30 sec. Blow dry with a compressed N_2 gun. Step 2.10 should be performed as soon as possible to prevent the native oxide from reappearing.

10. Use an e-beam evaporator to deposit 25 nm of Ni, 55 nm of Ge, and 80 nm of Au. The deposition rates are respectively 0.2 nm/sec, 0.5 nm/sec and 0.5 nm/sec. The deposition rates are chosen so that the evaporation time is short enough to avoid heating the chamber without being so short as to lose precision of the thickness of the deposited layer. The bilayer of Ge and Au can be replaced by a single layer of eutectic GeAu if it is available[9].

11. The previous step deposited metal on the entire surface of the sample. Removal of the metal that is deposited on the resist is done by dissolving the latter. To do this, immerse the sample in 1165 Remover at 65 °C for 3 hr. To remove any unwanted metal that may not have lifted on its own, use a pipette to lightly spray the surface of the sample with hot remover. Rinse the sample in acetone and IPA for 5 min each.

12. A rapid thermal anneal process in forming gas is used to diffuse the deposited metal down to the 2DEG of the sample. The temperature is increased at a rate of 50 °C/sec until a temperature of 415 °C is reached. The sample is left at this temperature for 20 sec and is then cooled down rapidly. The duration and the temperature of the anneal are chosen to obtain the smallest resistance through the ohmic contacts at low temperature. The optimal anneal time can vary depending on the depth of the 2DEG in the substrate.

3. Fabrication of the Ti/Au Schottky Leads

*The result of this fabrication step is shown in **Figure 4c**.*

1. Clean the sample in a sonic bath by immersion in acetone (2x) and IPA for 5 min each. Blow dry with a compressed N_2 gun.
2. Bake the sample in an oven at 125 °C for 15 min to dehydrate the surface.
3. Spin coat PMMALMW4% at 5000rpm for 30 sec and bake on a hot plate at 180 °C for 90 sec. Then, spin coat PMMA HMW 2% at 5,000 rpm for 30 sec and bake on a hot plate at 180 °C for 90 sec. The resulting thicknesses of resist are ~75 nm and ~40 nm, respectively. Since the Ti/Au leads will be very thin, a single layer of PMMA can be used, but spinning, exposure and development parameters will need to be adjusted in consequence. This comment also applies to the Al leads and gates (step 4).
4. **E-beam process:** *This part of the process is highly dependent on the equipment used and the protocol needed can thus differ greatly from the one described below. The patterns for the leads are drawn in a CAD file. In this file, the leads must be drawn as closed polygons that are 2 µm wide. The leads are needed to contact the bonding pads (fabricated in step 5) to the Al gates (fabricated in step 4). Four alignment marks must also be exposed to allow the vertical, horizontal, and rotational alignment of the Al leads and gates onto the Ti/Au Schottky leads.*
   1. Place the sample in a Scanning Electron Microscope (SEM) that is equipped to do e-beam lithography. Use an aperture of 10 µm to reduce the beam spot size and set the acceleration voltage to 10 kV to ensure a good contrast during the alignment on the previously fabricated structures. Adjust the focus, stigmatism, and the aperture alignment. Measure the beam current with a Faraday cup.
   2. Align the beam with the previously etched mesa and set the magnification to 300X.
   3. Expose the leads. The SEM is programmed to expose the desired areas by filling them with an array of exposed dots. The distance between these dots (center-to-center distance) is 5.5 nm and the dose is 43 µC/cm^2 (the exposure time will depend on the beam current measured in step 3.5.1). Expose alignment marks as well to allow the alignment of the Al gates with the Ti/Au leads in step 4.
   4. Repeat steps 3.5.2 and 3.5.3 for each of the 20 devices on the sample.

5. Develop the resist by immersing the sample in IPA:H_2O (9:1) for 30 sec. The solution must be at a temperature of 20 °C. Rinse in water for 30 sec and blow dry with a compressed N_2 gun. If preferred, the PMMA resist can be developed using an IPA:MIBK solution and rinsing in IPA to stop the reaction. A different development time will be needed if this option is chosen.

6. Place the sample in a plasma asher and expose it to an O_2 plasma for 4 sec at 50 W. This removes 5 nm of resist and ensures that there is no resist left at the bottom of the trenches formed during the e-beam process.

7. Remove the GaAs native oxide by immersing the sample in a solution of H_2SO_4:H_2O (1:5) for 30 sec and rinse in water for 30 sec. Blow dry with a compressed N_2 gun. Step 3.8 should be performed as soon as possible to prevent the native oxide from reappearing.

8. Place the sample in an e-beam evaporator and deposit 10 nm of Ti and 20 nm of Au, both at a rate of 0.1 nm/sec. It is important for the sample holder to be well grounded and placed at least 60 cm away from the source to prevent charges from accumulating on the sample during the deposition process.

9. Lift-off excess metal by immersing the sample in 1165 Remover at 65 °C for 15 min. To remove any unwanted metal that may not have lifted on its own, use a pipette to lightly spray the surface of the sample with hot remover. Rinse in acetone and IPA for 5 min each.

4. Fabrication of the Al Schottky Leads and Gates

*The result of this fabrication step is shown in **Figure 4d**.*

The fabrication of the Al Schottky leads and gates constitutes the most critical step of the fabrication process since these are the gates that define the dot. It is important that the electron beam be well focused and the beam current well adjusted in step 4.2. The exposure and development times must also be well adjusted to obtain small, continuous and well-defined gates. In many protocols, these gates and leads are fabricated in Ti/Au and are exposed simultaneously with the previous leads during step 3. However, an advantage of using Al is that it can be

oxidized, therefore allowing for elements such as top gates to be deposited directly onto the surface of the sample without the need of a large insulating layer[10].

1. Repeat steps 3.1 to 3.4.2. However, do not use the sonic bath while cleaning the sample to avoid damaging the Ti/Au leads.
2. **E-beam process**: The patterns for the Al leads and gates are drawn in a CAD file. The Al leads are used to contact the Ti/Au leads to the Al gates and are drawn as closed polygons with a width of 200 nm. The Al gates however are not drawn as polygons, but rather as two single lines separated by 20 nm.
   1. Once the beam has been aligned with the mesa, set the magnification to 1,500X and align the beam with the Ti/Au Schottky leads.
   2. Expose the leads. Use a dose of 43 $\mu C/cm^2$ and a center-to-center distance of 3.3 nm.
   3. Expose the gates. Use a line dose of 0.149 nC/cm and a center-to-center distance of 1.1 nm. This will lead to a final gate width of 60 nm.
   4. Repeat steps 4.2.1 - 4.2.3 for each of the 20 devices on the sample.

3. Repeat steps 3.5 - 3.7.
4. Place the sample in an e-beam evaporator and deposit 30 nm of Al at a rate of 0.3 nm/sec.
5. Repeat step 3.10. It is important to be very delicate with the sample from this step onward to avoid damaging the small Al gates.

5. Fabrication of the Schottky Leads and Bonding Pads

*The result of this fabrication step is shown in **Figure 4e**.*

1. Repeat steps 2.1 - 2.9, using a photolithographic mask for the Schottky leads instead of the mask for the ohmic pads.
2. Place the sample in an e-beam evaporator and deposit 30 nm of Ti and 350 nm of Au at rates of 0.3 nm/sec and 1 nm/sec respectively. The thick layer of Au deposited facilitates bonding of the sample to the sample holder because it is less prone to tearing than thinner layers.
3. Lift-off the excess metal and remaining resist by immersing the sample in 1165 Remover at 65 °C for 3 hr. To remove any unwanted metal that may not have lifted on its own, use a pipette to lightly spray the surface of the sample with hot remover. Rinse the sample in acetone and IPA for 5 min each.

6. Dicing of the Samples

1. Bake the sample in an oven at 125 °C for 15 min to dehydrate the surface.
2. Spin coat with S1818 at 3,500 rpm for 30 sec and bake on a hot plate at 115 °C for 1 min. The thickness of this layer of resist is unimportant as long as it is thick enough to protect the surface of the sample during dicing.
3. Place a layer of dicing tape on the top and bottom faces of the sample. The layer of tape on the top face offers an additional layer of protection to the device during dicing.
4. Place the sample face-up in a dicer. Cut the sample into individual devices by dicing all the way through top layer of dicing tape and the GaAs/AlGaAs wafer without cutting through the bottom layer of dicing tape.
5. Remove the dicing tape and the protective resist by placing the sample in acetone for a few minutes. Use tweezers to gently pull off pieces of dicing tape that do not lift on their own. Rinse the devices in IPA and blow dry using an N_2 gun.

Representative Results

One of the critical steps in the process described above is the etching of the mesa (step 1). It is important to etch enough to remove the 2DEG below while avoiding overetching. Therefore, it is recommended to use a bulk GaAs dummy sample to test the etching solution before performing the etch on the GaAs/AlGaAs sample. The etch rate of the GaAs/AlGaAs heterostructure is larger than that of GaAs, but the etching of the dummy can give an indication to whether the solution is more or less reactive than usual and the etch time of the actual sample can be adjusted accordingly.

Once the devices have been fabricated, they are ready to be attached to a sample holder using silver epoxy. Wire bonding between the sample's bonding pads and the sample holder's connection pins is done using 25 μm Al wire. It is best to avoid observing the devices in a Scanning Electron Microscope (SEM) because there is a risk of damaging them. Instead, there are simple tests that can be done at fairly high temperatures (~4 K) and that allow to confirm if any of the gates are broken or missing before cooling the sample in a dilution refrigerator for further characterization. One of these tests consists in applying a voltage bias between two ohmic contacts and measuring the current driven through the sample as a function of the voltage applied on a pair of gates. An example of such measurements is shown in **Figure 5**. The curves in **Figure 5** show two distinct regimes. The first regime ranges from 0 V to -750 mV and presents two depletion steps: one at about -300mV corresponding to the depletion of the 200 nm wide leads and one at about -750mV corresponding to the depletion of the 60 nm wide gates. The second regime at lower voltages shows plateaus that correspond to the quantization of the conductance. Typical values for pinch-off points between pairs of gates range between -500mV to -2V. Moreover, one shouldn't apply positive voltage above 500 or 600 mV on a gate since it could damage the Schottky barrier. From **Figure 5**, it is possible to conclude that, in the case of this particular sample, the gates are likely to be geometrically similar since the TC-TL and TC-TR pairs pinch off the current at approximately equal voltages. The same goes for the TC-BL and TC-BR pairs. However, the fact that the current still flows between the TC and BC gates even for high voltages indicates that the BC gate is either broken or missing. Usually, about 50% of the tested devices have fully functional gates and ohmic contacts.

Once a suitable device has been found, it can be loaded into a dilution refrigerator for characterization at low temperatures (<100 mK). The voltages on each of the gates must then be adjusted to form the double dot. It is not the goal of this paper to detail this adjustment process. Once a double dot has been formed, a stability diagram can be measured to check if the double dot can reach the few-electron regime. This is done by applying a small constant source-drain bias (~10 μV) and by measuring the current through the double dot as a function of the voltages applied on the BL and BR gates. If the design of the device includes a quantum point contact which serves as a charge detector, it is preferable to use

this, rather than the current through the dot, for the measurement of the stability diagram[11]. A measured stability diagram and a schematic of an ideal result are shown in **Figure 6**. As shown in **Figure 6b**, current only flows through the double dot at triple points. The zero-electron regime is reached when no more triple points can be observed in the stability diagram, no matter how negative the voltages on the gates become. However, the fact that current no longer flows through the dot for high voltages can also indicate that the tunnel barriers connecting the source and drain to the double dot have been completely pinched off. Spin blockade can be measured at different triple points to prove that the few-electron regime has been reached[12], but the exact number of electrons in the double dot needs to be determined using charge sensing. For more detailed information regarding stability diagrams, spin blockade and charge sensing see R. Hanson *et al*.[13]
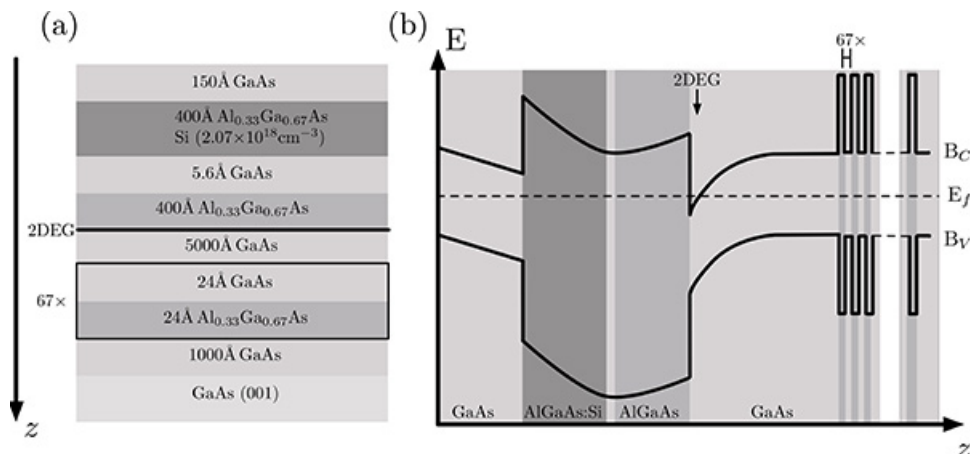

Figure 1. a) Sequence of layers present in a GaAs/AlGaAs heterostructure grown by molecular beam epitaxy. b) Band structure of the heterostructure shown in **a)**. B_c and B_v are respectively the conduction and valence bands. The only region where the conduction band is below the Fermi level (E_f) is found between the 5,000 Å layer of GaAs and the 400 Å layer of AlGaAs. It is here that the 2DEG is found. Click here to view larger image.
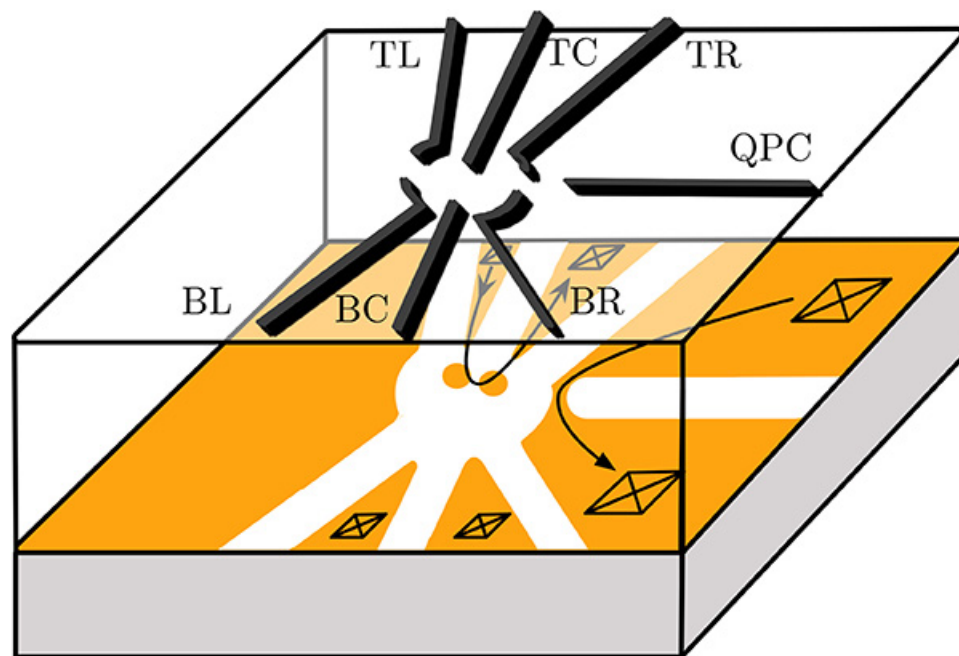

Figure 2. Schematic of the metallic gate electrodes (dark grey) of a double quantum dot deposited on top of a GaAs/AlGaAs heterostructure. The 2DEG is shown in orange and the depleted regions are white. The black squares represent ohmic contacts and the arrows show the current flow through the dot and the quantum point contact (QPC). The two dots are located in the orange regions where electrons still remain in the center of the depleted zone. Gates BL and BR are used to control the number of electrons on the left and right dots respectively. BC and TC control the tunnel barrier between the two dots. TL is used to tune the tunnel barrier between the source and the left dot while TR tunes the barrier between the right dot and the drain. Click here to view larger image.
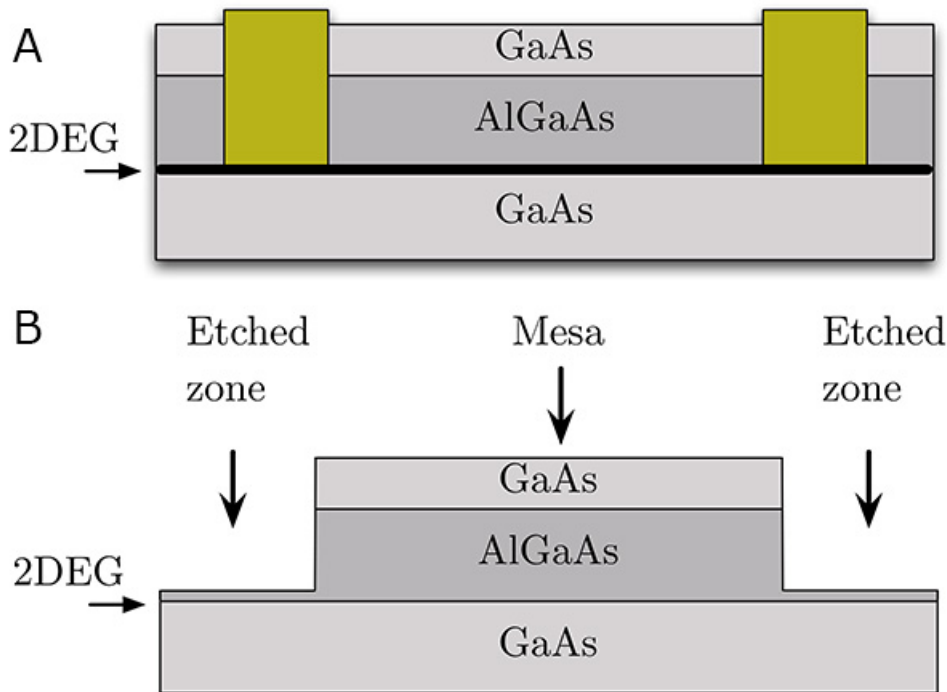
Figure 3. (a) Schematic of a Ni/Ge/Au ohmic contact (golden rectangles) diffused by rapid thermal anneal from the surface of the sample down to the 2DEG. (b) Lateral view of the surface of the sample that is etched to create the mesa. Click here to view larger image.
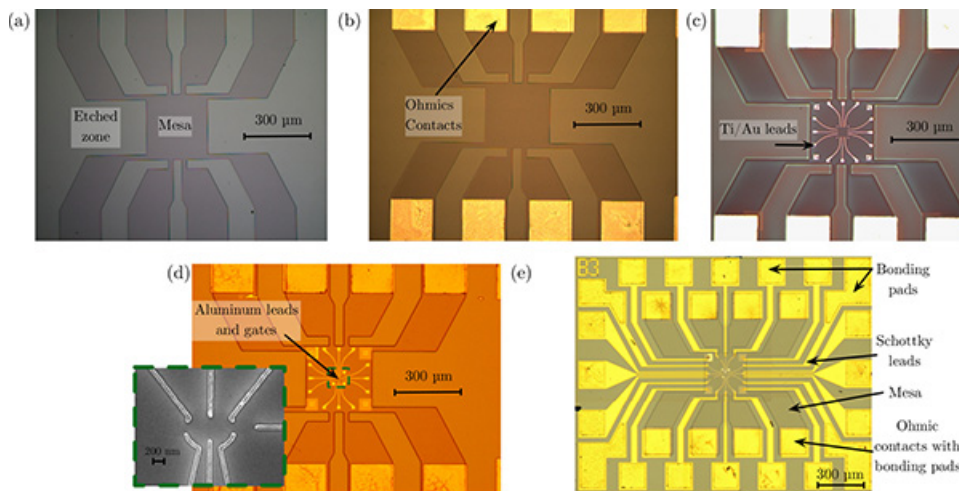
Figure 4. Optical microscope images of a double quantum dot device after different steps of the fabrication process. (a) Device after the etching of the mesa (step 1). The light gray areas have been etched away preventing the electric current from flowing through these regions, while the dark gray regions still present a 2DEG. **(b)** Device after the fabrication of the ohmic contacts (step 2). The ohmic contacts are the gold squares. **(c)** Device after the fabrication of the Ti/Au Schottky leads (step 3). The leads are the white lines in the center of the image. **(d)** Device after the fabrication of the Al Schottky leads and gates (step 4). These are found in the green square in the center of the image. A SEM image of the gates used to define the quantum dots is also shown. **(e)** Device after the fabrication of the Schottky leads and bonding pads (step 5). Click here to view larger image.
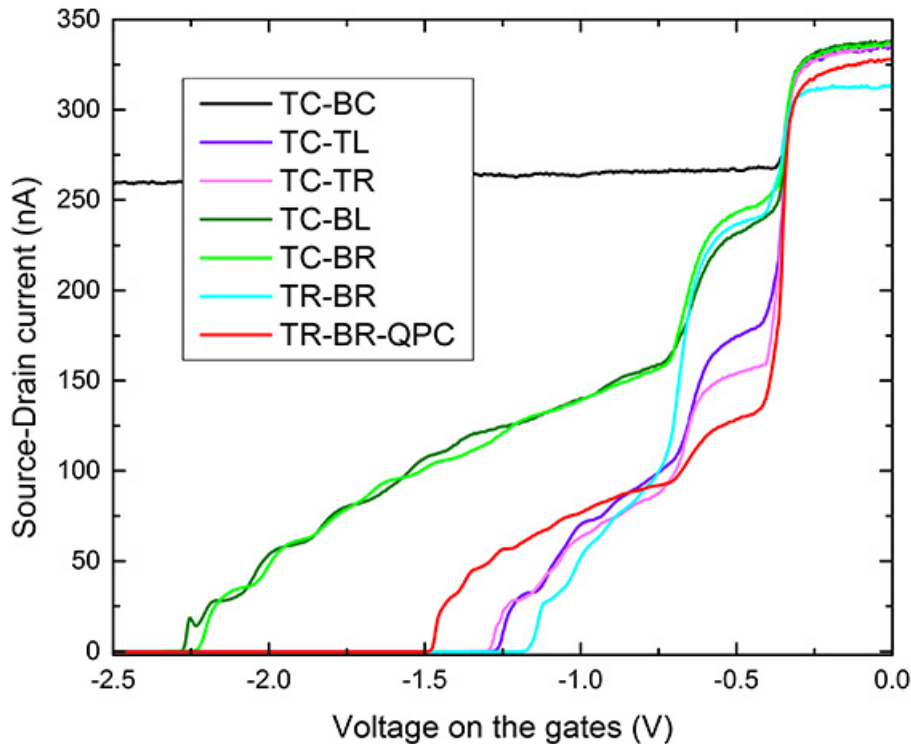
Figure 5. Current flowing from source to drain as a function of the voltage applied on different pairs of gates. The depletion of the electron gas begins at ~-400 mV and is finished at ~-700 mV. The voltage bias applied between the source and the drain is 500 µV and the current is measured by a two-point measurement. All curves are taken at 1.4 K. Click here to view larger image.
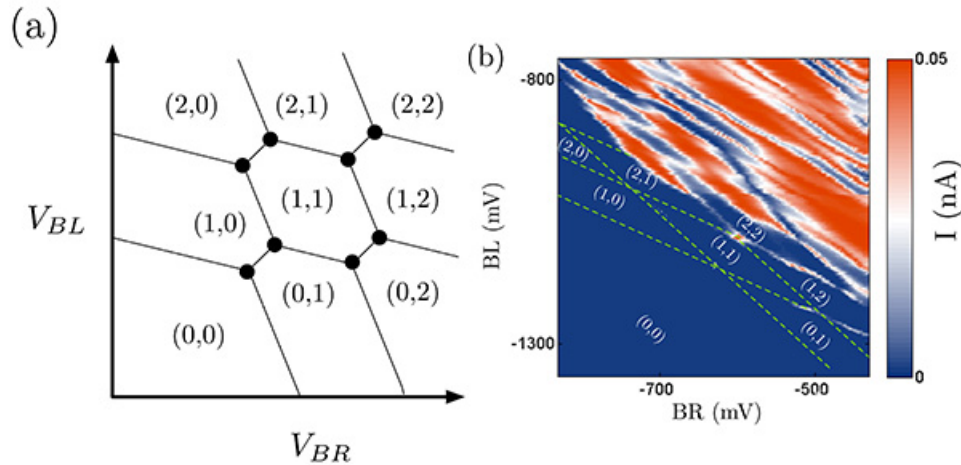
Figure 6. (a) Schematic of an ideal stability diagram that would be obtained using a QPC. Lines can be observed when an electron tunnels onto one dot or between the dots. The black circles represent triple points where it is possible for current to flow through the dot. **(b)** Stability diagram obtained by measuring the current flowing through the dot with TL = -100 mV, TC = -350 mV, TR = -1,080 mV, BC = -1,160 mV, QPC = -600 mV and a source-drain bias of 10 µV. The sample was bias-cooled with a voltage V = +500 mV on each gate, which shifts all the depletion and pinch-off points by approximately 500 mV and reduces telegraphic noise in the experiment[14]. For this type of stability diagram, only the triple points are supposed to be visible, as is the case here for the most negative voltages. In both **(a)** and **(b)**, the numbers (L,R) indicate the number of electrons in the left and right dot for different values of the voltages on the BL and BR gates. The green lines in **(b)** are guides to show the regions with a constant number of electrons. Click here to view larger image.

Discussion

The process presented above describes the fabrication protocol of a double quantum dot able to reach the few-electron regime. However, the parameters given may vary depending on the model and calibration of the equipment used. Therefore, parameters such as the doses for exposures during the e-beam and photolithography steps will have to be calibrated before the fabrication of devices. The process can easily be adapted to the fabrication of gate-defined quantum dots on other types of substrates, such as Si/SiGe, that also present a 2DEG.

For certain types of devices, such as vertical quantum dots, the tunnel barrier from the source and the drain to the dot are determined during fabrication and cannot be varied afterward[5]. An advantage of gate-defined lateral quantum dots is that the tunnel barriers to the dot as well as between the dots can be controlled electrically. However, because of this, care must be taken to maintain these values during the manipulation of the voltages on the other gates defining the dot.

It is important to remember that, once the few-electron regime has been reached, the goal is to manipulate the spin states of the electrons on the dot to perform quantum calculations. The 0 and 1 states of the qubit have been successfully implemented in the up and down spin states of a single electron[15] as well as in the S-T_0[16] and S-T_+[17] states of two spins. Coupling between two qubits has also been achieved using these devices[18]. However, one of the major drawbacks of lateral quantum dots in GaAs/AlGaAs is the short coherence time (the time during which the spin state of the electrons in the dot is preserved) caused by interaction with the nuclear spins of the atoms forming the substrate[19]. This has led to the investigation of lateral quantum dots in materials such as silicon (Si/SiGe heterostructures[20]) and carbon (graphene[21]) that have isotopes that are free of nuclear spin and are expected to lead to theoretically long coherence times. However, these devices have yet to achieve the results of control and read-out obtained for dots in GaAs/AlGaAs. Current work involving GaAs/AlGaAs double quantum dots also includes coupling of the device to a microwave resonator[22] and the integration of micromagnets to allow faster spin operations[23].

Disclosures

Authors have nothing to disclose.

Acknowledgements

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