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Epitaxial Nanostructured α-Quartz Film on Silicon: From the Material to New Devices

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Abstract

In this work, we show a detailed engineering route of the first piezoelectric nanostructured epitaxial quartz-based microcantilever. We will explain all the steps in the process starting from the material to the device fabrication. The epitaxial growth of α-quartz film on SOI (100) substrate starts with the preparation of a strontium doped silica sol-gel and continues with the deposition of this gel into the SOI substrate in a thin film form using the dip-coating technique under atmospheric conditions at room temperature. Before crystallization of the gel film, nanostructuration is performed onto the film surface by nanoimprint lithography (NIL). Epitaxial film growth is reached at 1,000 °C, inducing a perfect crystallization of the patterned gel film. Fabrication of quartz crystal cantilever devices is a four-step process based on microfabrication techniques. The process starts with shaping the quartz surface, and then metal deposition for electrodes follow it. After removing the silicone, the cantilever is released from SOI substrate eliminating SiO_2 between silicon and quartz. The device performance is analyzed by non-contact laser vibrometer (LDV) and atomic force microscopy (AFM). Among the different cantilever's dimensions included in the fabricated chip, the nanostructured cantilever analyzed in this work exhibited a dimension of 40 µm large and 100 µm long and was fabricated with a 600 nm thick patterned quartz layer (nanopillar diameter and separation distance of 400 nm and 1 µm, respectively) epitaxially grown on a 2 µm thick Si device layer. We measured a resonance frequency at 267 kHz and the estimated quality factor, Q, of the whole mechanical structure was Q ~ 398 under low vacuum conditions. We observed nanometric linear dependence of cantilever displacement and applied AC voltage with both techniques (i.e., AFM contact measurement and LDV). Therefore, proving that these devices can be activated through the indirect piezoelectric effect.

Introduction

Oxide nanomaterials with piezoelectric properties are pivotal to design devices such as MEMS sensors or micro energy harvesters or storage[1,2,3]. As the advances in CMOS technology increase, the monolithic integration of high-quality epitaxial piezoelectric films and nanostructures into silicon becomes a subject of interest to expand new novel devices[4]. In addition, greater control of miniaturization of these devices is required to achieve high performances[5,6]. New sensor applications in electronic, biology, and medicine are enabled by the advances in micro and nanofabrication technologies[7,8].

In particular, α-quartz is widely used as a piezoelectric material and shows outstanding characteristics, which allow users to make fabrication for different applications. Although it has low electromechanical coupling factor, which limits its application area for energy harvesting, its chemical stability and high mechanical quality factor make it a good candidate for frequency control devices and sensor technologies[9]. However, these devices were micromachined from bulk single quartz crystals which have the desired characteristics for device fabrication[10]. The thickness of the quartz crystal should be configured in such a way that the highest resonance frequency can be obtained from the device, nowadays, the lowest achievable thickness is 10 μm[11]. So far, some techniques to micropattern the bulk crystals such as Faraday cage angled-etching[11], laser interference lithography[12], and focused ion beam (FIB)[13] were reported.

Recently, direct and bottom-up integration of epitaxial growth of (100) α-quartz film into silicon substrate (100) was developed by chemical solution deposition (CSD)[14,15]. This approach opened a door to overcome the aforementioned challenges and also to develop piezoelectric-based devices for future sensor applications. Tailoring the structure of α-quartz film on silicon substrate was achieved and it allowed to control the texture, density, and the thickness of the film[16]. The thickness of the α-quartz film was extended from a few hundred nanometers to the micron range, which are 10 to 50 times thinner than those obtained by top-down technologies on bulk crystal. Optimizing the dip-coating deposition conditions, humidity and temperature was enabled to attain both continuous nanostructured crystalline quartz film and a perfect nanoimprinted pattern by a combination of a set of top-down lithography techniques[17]. Specifically, soft nanoimprint lithography (NIL) is a low-cost, large-scale fabrication and benchtop equipment-based process. Application of soft NIL, which combines top-down and bottom-up approaches, is a key to produce epitaxial quartz nanopillar arrays on silicon with a precise control of pillar diameters, height, and the interpillar distances. Furthermore, fabrication of silica nanopillar with controlled shape, diameter, and periodicity on borosilicate glass for a biological application was performed customizing soft NIL of epitaxial quartz thin film[18].

Up to now, it has not been possible for on-chip integration of piezoelectric nanostructured α-quartz MEMS. Here, we draw the detailed engineering route starting from material to device fabrication. We explain all the steps for material synthesis, soft NIL, and the microfabrication of the device to release a piezoelectric quartz cantilever on SOI substrate[19] and discuss its response as a piezoelectric material with some characterization results.

Protocol

1. Preparation of the solution

1. Prepare a solution containing prehydrolyzed tetraethyl orthosilicate (TEOS) 18 h before the production of the

gel films in a fume hood in which a lab balance and a magnetic stirrer are placed.

1. Add 0.7 g of polyethylene glycol hexadecyl ether (Brij-58) and 23.26 g of ethanol into 50 mL bottle and close the lid of the bottle and stir it until the Brij is completely dissolved.
2. Add 1.5 g of HCl 35% into the flask in step 1.1.1, close it and stir for 20 s.
3. Add 4.22 g of TEOS to the flask in step 1.1.2, close it and let it stir for 18 h.

2. Preparation of 1 M aqueous solution of Sr^{2+} just before the production of the gel films because a matured solution is susceptible to re-precipitate in form of Sr salt.
   1. Weigh 2.67 g of $SrCl_2 \cdot 6H_2O$ in a 10 mL volumetric flask.
   2. Add 10 mL ultrapure water (e.g., Milli-Q) up to 10 mL into the flask in step 1.2.1 and close the flask with a plastic cap and gently shake the flask to dissolve the strontium chloride.
3. Add 275 µL of the 1 M aqueous solution of Sr^{2+} into the 10 mL bottle containing the solution that was prepared in step 1.1 and stir the solution for 10 min.

2. Preparation of polydimethylsiloxane (PDMS) templates

1. Preparation of PDMS solution after step 1.3.
   1. Mix 1 part of the curing agent with 10 parts of the elastomer in a beaker on the balance. Stir the mixture with a glass stick until obtaining a homogeneous distribution of bubbles and remove it in a vacuum chamber.
2. Replicate the silicon master using the PDMS solution. Notice that for this work, we used a silicon patterned master composed of pillars with diameters, height, and separation distance of 1 µm.
   1. Put the silicon master with the structured face up in a plastic box and fill the box with the PDMS solution.
   2. Introduce the plastic box into the furnace at 70 °C for 2 h to obtain a solid PDMS template.
   3. Separate the PDMS template and the silicon master. Cut the PDMS template to the desired size using a blade and keep it in a clean box.

3. Gel film deposition on SOI (100) substrates by dip-coating

1. Preparation of the substrates
   1. Prepare 2 cm x 6 cm sized substrates by cutting a 2-inch p-type SOI wafer with the thickness of 2/0.5/0.67 µm ($Si/SiO_2/Si$) in a direction parallel or perpendicular to the wafer flat using a diamond tip. Notice that the conductivity of the silicon device layer must be between 1 and 10 Ω/cm.
   2. Introduce substrates in a piranha solution for 20 min in order to eliminate possible fabrication polymers.
   3. Clean with pure water, then with ethanol, and let them dry or use nitrogen flow. This step should be performed just after step 1.3.
2. Deposition of a solution containing pre-hydrolyzed tetraethyl orthosilicate (TEOS), Brij-58 sulfactant and $SrCl_2$ $6H_2O$.
   1. In order to obtain a homogeneous silica film, set the dip-coater's chamber under the conditions at relative humidity 40% and 25 °C of temperature.

2. Place a beaker with the size of around 5 cm x 1 cm x 8 cm underneath the SOI substrate hanging from the dip-coater arm and establish a dip coating sequence with the speed of 300 mm/min at the immersion and withdrawal. Set the immersion time (time at the final position) to zero.
3. Fill the beaker with the solution prepared in step 1.3 and wait until the relative humidity temperature becomes stable, i.e., 40% and 25 °C, respectively.
4. Perform a single dip coating and wait until the film becomes homogeneous.
5. Introduce the SOI substrate into a furnace at 450 °C for 5 min to consolidate de-gel film obtaining a thickness of 200 nm.
6. Repeat steps 3.2.3 and 3.2.4 two times more to produce a film with around 600 nm of thickness. To ensure the stability of the solution, a repeating process should be performed in 1 h.

4. Surface micro/nanostructuration by soft imprint lithography

1. Prepare the micro/nano structures on the film surface under the conditions of relative humidity 40% and 25 °C of temperature.
    1. Repeat step 3.2.3 to deposit a new film on SOI substrate.
    2. Place the SOI substrate after step 3.2.1 on a flat surface and put the PDMS mold prepared in step 2.2 on the SOI substrate while the sol-gel is evaporating.
    3. Put the SOI substrate with the PDMS mold in a furnace at 70 °C for 1 min, and then at 140 °C for 2 min in a second furnace. Then, leave it for cooling down.
    4. Remove the PDMS mold to obtain a micro/nanostructured gel film on the SOI substrate.
    5. Introduce the SOI substrate into a furnace at 450 °C for 5 min to consolidate a micro/nanostructured gel film 600 nm height.

5. Gel film crystallization by thermal treatment

1. Thermal treatment of the gel films on SOI (100).
    1. Program the tubular furnace heating from room temperature to 1,000 °C
    2. Introduce the sample placed in a ceramic boat into the furnace at 1,000 °C for 5 hours. Do not cover the tubular working tube during the whole thermal treatment in order to saturate the furnace with air. Finally, reach the room temperature by cooling the furnace without any programmed ramp.

6. Designing of lithography mask layout

The mask used in this process is designed specifically for a device fabrication on the SOI substrate with epitaxial nanostructured quartz. All the fabrication processes are carried out on the quartz side. The mask was designed in a way that negative tone resist needs to be used in each step. The mask is organized in four different steps as explained below.

1. Patter the quartz to determine the shape of the cantilever and also 30 µm x 30 µm square shape contact area. For example, 40 µm x 100 µm size rectangular shape cantilever area out of 120 µm x 160 µm area is protected with negative resist and the rest is etched until silicon layer.

2. Realize the top and bottom electrodes. Top electrode is patterned on the rectangular shaped cantilever area and the bottom electrode is patterned on the 2 µm thick silicon layer on the 30 µm x 30 µm etched area. The width of the top contact is 4 µm smaller than the patterned cantilever area and the size of the bottom contact is bigger than the 30 µm x 30 µm square shape etched area in step 1.
3. Etch all the 2 µm thick silicon layers in 120 µm x 160 µm U-shaped area around the rectangle-shaped cantilever. The etched area is again U-shaped but 4 µm smaller from each side to protect the cantilever area from HF attack in the last step.
4. Release the cantilever with BOE etching of SiO_2. The protected cantilever area is 2 µm bigger than the actual cantilever area. The most important part is to protect the surface and blanks of the cantilever.

7. Cleaning of the quartz samples for the cantilever microfabrication process with piranha solution

1. Prepare a piranha solution by slowly adding 10 mL of hydrogen peroxide (H_2 into 20 mL of sulfuric acid (H_2SO_4) at ambient temperature. This mixture creates a thermal reaction.
    1. Put the samples inside this solution for 10 min in order to clean all the organic residues.
    2. Rinse the samples with DI water and dry them with nitrogen.

8. Step 1: Patterning cantilever shape on the quartz thin film

1. The first lithography process
    1. Rinse the samples with acetone, IPA, and then blow dry with nitrogen.
    2. Put the samples on the hot plate at 140°C for 10 min of dehumidification.
    3. Spin AZ2070 negative photoresist at a speed of 4,000 rpm for 30 s.
    4. Put the samples on the hot plate to softbake at 115 °C for 60 s.
    5. Expose the sample with 37.5 $mJ.cm^{-2}$ UV dose for 5 s.
    6. Put the sample on the hot plate for post exposure bake at 115 °C for 60 s.
    7. Develop in MIF 726 developer for 100 s at ambient temperature, then rinse in DI water and blow dry with nitrogen. The expected thickness is 5.5 µm.
    8. Put the sample on the hotplate at 125 °C for 10 min to hardbake the resist.
2. Reactive Ion Etching (RIE) of the quartz layer
    1. Etch the quartz until silicon layer using RIE with a gas flow rate of 60 sccm CHF_3, 20 sccm 0_2, and 10 sccm Ar at 100 W RF power.
3. Cleaning the resist residuals
    1. Clean with plasma at a flow rate of 90 sccm 0_2 for 5 min.
    2. If the first cleaning step is not enough, leave the sample in remover PG at 80 °C until all the resists are removed.
    3. Then, put the sample in a piranha solution (20 mL of sulfuric acid H_2SO_4 + 10 mL of hydrogen peroxide

H_2 for 10 min. Then, rinse in DI water and blow dry with nitrogen.

9. Step 2: Realization of bottom and top electrode

1. The second lithography process
    1. Rinse the samples with acetone, IPA, and then blow dry with nitrogen.
    2. Put the samples on the hot plate at 140 °C for 10 min of dehumidification.
    3. Spin AZ2020 negative photoresist at a speed of 4,000 rpm for 30 s.
    4. Put the sample on the hot plate to softbake at 115 °C for 60 s.
    5. Expose the sample with 23.25 $mJ.cm^{-2}$ UV dose for 3 s.
    6. Put the sample on the hot plate for post exposure bake at 115 °C for 60 s.
    7. Develop in MIF 726 developer for 50 s at ambient temperature, then rinse in DI water and blow dry with nitrogen. The expected thickness is 1.7 µm.
2. Metal deposition for top and bottom electrodes.
    1. Deposit 50 nm Chromium at a rate of 4 A/s and 120 nm Platinum at 2.5 A/s with electron beam evaporation at 10^{-6} mbar.
3. Metal lift-off
    1. Leave the samples firstly in acetone and then in IPA until metal lift off is successful.
    2. Check the sample with an optical microscope and if necessary, leave the sample in remover PG at 80 °C until all metals lift-off. Then, rinse in DI water and blow dry with nitrogen.
    3. If step 9.3.2 is not enough, put the samples in an ultrasonic cleaner in acetone for 5 min. Repeat this operation as many times as necessary.
    4. Rinse the samples with acetone, IPA, and then blow dry with nitrogen.

10. Step 3: Patterning the sample to etch Si(100) layer

1. The third lithography process
    1. Rinse the samples with acetone, IPA, and then blow dry with nitrogen.
    2. Put the samples on the hot plate at 140 °C for 10 min of dehumidification.
    3. Spin AZ2070 negative photoresist at a speed of 2,000 rpm for 30 s.
    4. Put the sample on the hotplate for softbake at 115 °C for 60 s.
    5. Expose the sample with 37.5 $mJ.cm^{-2}$ UV dose for 5 s.
    6. Put the sample on the hotplate for post exposure bake at 115 °C for 60 s.
    7. Develop in MIF 726 for 110 s at ambient temperature, then rinse in DI water and blow dry with nitrogen. The expected thickness is 5.9 µm.
    8. Put the sample on the hot plate at 125 °C for 10 min to hardbake the resist.
2. Reactive Ion Etching of the silicon layer
    1. Etch the silicon layer until Si layer using RIE with gas flow rate of 60 sccm CHF_3, 20 sccm 0_2 and 10 sccm Ar at 100W RF power.
3. Cleaning the resist residuals

1. First clean with plasma at a flow rate of 90 sccm 0_2 for 5 min.
2. Leave the sample in remover PG at 80 °C until all resists are removed. Then, rinse in DI water and blow dry with nitrogen.

11. Step 4: Releasing cantilever by wet chemical etching of SiO_2

1. The fourth lithography process
    1. Rinse the samples with acetone, IPA, and then blow dry with nitrogen.
    2. Put the samples on the hot plate at 140 °C for 10 min of dehumidification.
    3. Spin AZ2020 negative photoresist at a speed of 2,000 rpm for 30 s.
    4. Put the sample on the hotplate for soft bake at 115 °C for 60 s.
    5. Expose the sample with 37.5 $mJ.cm^{-2}$ UV dose for 5 s.
    6. Put the sample on the hotplate for post exposure bake at 115 °C for 60 s.
    7. Develop in MIF 726 for 65 s at ambient temperature. Rinse in DI water and then blow dry with nitrogen. The expected thickness is 2.3 µm.
    8. Put the sample on the hotplate at 125 °C for 10 min to hardbake the resist.
2. Wet etching of SiO_2 layer with buffered oxide etch (BOE)
    1. Put BOE 7:1 solution in a polytetrafluoroethylene (PTFE) based container.
    2. Put the sample in this solution and leave it at ambient temperature until all SiO_2 layers are etched under the cantilever. Then rinse in DI water and blow dry nitrogen.
3. Cleaning the resist residuals
    1. Rinse the samples with acetone, IPA, and then blow dry with nitrogen.
    2. If necessary, clean the resist residuals with plasma at a flow rate of 90 sccm O_2 for 5 min.

Representative Results

The progress of the material synthesis and device fabrication (see **Figure 1**) was depicted schematically by monitoring different steps with real images. After the microfabrication processes, we observed the aspect of the nanostructured cantilevers using the field emission Scanning Electron Microscopy (FEG-SEM) images (**Figure 2a-c**). 2D Micro X-ray diffraction controlled the crystallinity of the different stacking layers of the cantilever (**Figure 2d**). We also analyzed the detailed crystallization of quartz pillars using electron diffraction technique and FEG-SEM images in the backscattered electrons mode (**Figure 2e-f**). A deeper structural characterization of a single quartz-based piezoelectric nanostructured cantilevers was performed by recording the pole figure and rocking curve as shown in **Figure 2g-i**. The Electromechanical response of the quartz-based piezoelectric cantilevers was detected using both (i) a Laser Doppler Vibrometer (LDV) equipped with laser, photodetector and frequency generator (see **Figure 2j**) and (ii) an atomic force microscope in which the AC drive output of a Lock-in Amplifier (LIA) is fed to the top and bottom electrodes of the cantilever, while the vibration is recorded with the Optical Beam Deflection System of the AFM (see **Figure 2k,l**). Notice that the vibrometer was used in the displacement mode with a range of 50 nm/V. The frequency generator utilized to actuate the inverse-piezoelectricity of

quartz by the cantilever itself was an arbitrary waveform generator.

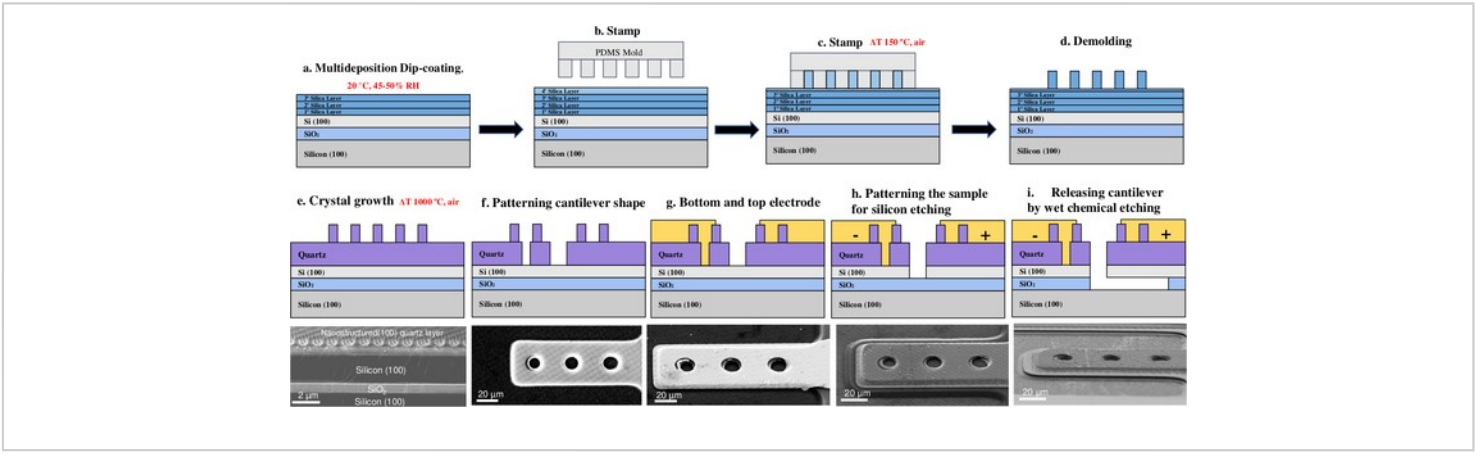

Figure 1: Device fabrication. General schematics and FEG-SEM images of the synthesis and microfabrication steps of quartz cantilever. (**a**) Dip coating multilayer deposition of Sr-silica solution on SOI substrate is followed by nanostructuring of the film with NIL process (**B,c,d**). (**e**) annealing of the sample at 1,000 °C in the air atmosphere enables the crystallization of nanostructured quartz film. Finally, a nanostructured quartz cantilever is fabricated with silicon micromachining (**f,g,h,i**).

Please click here to view a larger version of this figure.

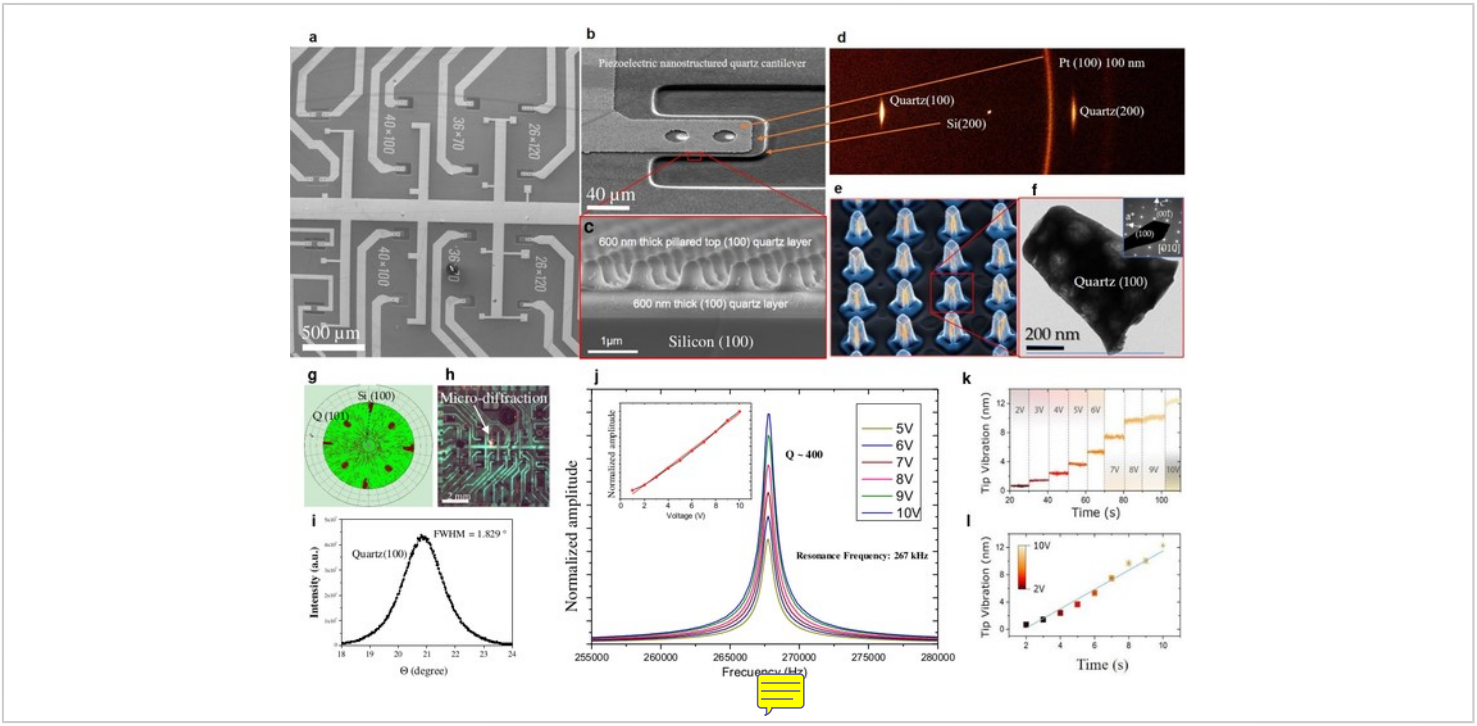

Figure 2: (**a**) SEM image of a nanostructured quartz-based chip with different cantilever dimensions. (**b**) SEM image of a single nanostructured quartz cantilever (36 µm large and 70 µm long). (**c**) Cross sectional FEG-SEM image of nanostructured quartz film on SOI substrate. (**d**) 2D X-ray diffraction pattern of the nanostructured cantilever. Notice that the different layers together with their thicknesses are indicated in the diffractogram. (**e**) FEG-SEM top image of nanostructured quartz film. (**f**) Higher resolution TEM image of a single quartz pillar. The inset shows the single crystal nature of the pillar resolved by electron diffraction. (**g**) 2D pole figure of α-quartz(100)/Si(100) cantilever. (**h**) Optical image of the whole chip during microdiffraction measurements pointed by a laser beam. Notice that the green color in the optical image corresponds to the diffraction of the natural light produced by the interaction of light and the quartz nanopillar that act as a photonic crystal. (**i**) Rocking curve of the quartz/Si cantilever showing a mosaicity value of 1.829° of the (100) quartz reflection. (**l**) Mechanical characterization by noncontact vibrometry measurements under low vacuum of a quartz-based cantilever of 40 µm large and 100 µm long composed of a 600 nm thick patterned quartz layer. The nanopillars diameter and separation distance are 400 nm and 1 µm, respectively and the thickness of the Si device layer is 2 µm. The inset image shows the linear dependence of the cantilever amplitude and applied AC voltage. (**k,l**) Atomic Force Microscopy measurements in which the AC drive output of a Lock-in Amplifier (LIA) is fed to the top and bottom electrodes of the sample, while the vibration is recorded with the Optical Beam Deflection System of the AFM, i.e., LIA's amplitude versus time for different applied voltage amplitudes (from 2 to 10 VAC). Notice that we observed similar linear dependence of the cantilever displacement in nanometers and applied AC voltage. Please click here to view a larger version of this figure.

Discussion

The presented method is a combination of bottom-up and top-down approaches to produce nanostructured piezoelectric quartz micro-cantilevers on Si. Quartz/Si-MEMS technology offers major advantages over bulk quartz in terms of size, power consumption, and integration cost. Indeed, epitaxial quartz/Si MEMS are produced with CMOS-compatible processes. This could facilitate the future fabrication of single chip solutions for multifrequency devices while preserving miniaturization and cost-effective processes. Compared to the current manufacturing of quartz devices, a top down technology based on cutting and polishing of large hydrothermally grown crystals, the method described in the protocol allows obtaining considerable thinner quartz layers on SOI substrate, with thicknesses between 200 and 1,000 nm and precise nanostructuration, which can generate piezoelectric patterned micro-devices of different dimensions and design. The dimensions of the quartz devices obtained by standard method cannot be below 10 µm thick and 100 µm in diameter and for most applications these need to be bonded on Si substrates. This feature limits the working frequencies and sensitivity of the current transducers.

The piezoelectric quartz devices obtained with the protocol could find applications in the near future in the field of electronics, biology, and medicine. Due to its coherent quartz/silicon interface, thicknesses below 1,000 nm and a controlled nanostructuration these are expected to present higher sensitivities while preserving the mechanical quality factor of the device. Moreover, it is envisioned that these devices will operate both (i) at low mechanical frequency of the MEMS structure, which depends on the device dimension, and (ii) at the intrinsic quartz material frequency, which depends on the thickness of the quartz, i.e., around 10 GHz for an 800 nm thick resonator[10]. A key aspect in order to obtain good quality cantilevers is ensuring the preservation of the crystal quality and piezoelectric functionality of the active quartz layer during the different lithographic processes. Indeed, a lithographic step process was created to protect the lateral edges of the nanostructured quartz layer to avoid any risk of HF acid infiltration during the release of the cantilever. As a result, the quartz/Si cantilever presents a uniform epitaxial crystallinity and piezoelectric properties of quartz, as indicated by the structural and resonance frequency characterization from 2D X-ray microdiffraction and non-contact vibrometer measurements.

Disclosures

The authors have nothing to disclose.

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