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Title: Epitaxial Nanostructured α-Quartz Film on Silicon: From the Material to New Devices

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Author Questionnaire

1. **Microscopy**: Does your protocol require the use of a dissecting or stereomicroscope for performing a complex dissection, microinjection technique, or something similar? **No**

2. **Software:** Does the part of your protocol being filmed include step-by-step descriptions of software usage? **No, just individual screenshots.**

3. **Interview statements:** Considering the COVID-19-imposed mask-wearing and social distancing recommendations, which interview statement filming option is the most appropriate for your group? **Please select one**.

   ☒ Interviewees wear masks until videographer steps away (≥6 ft/2 m) and begins filming, then the interviewee removes the mask for line delivery only. When take is captured, the interviewee puts the mask back on. Statements can be filmed outside if weather permits.

4. **Filming location:** Will the filming need to take place in multiple locations? **No, 2 labs in the same building**

Current Protocol Length

Number of Steps: 26
Number of Shots: 58

Introduction

1. Introductory Interview Statements

REQUIRED:

1.1. **Adrian Carretero:** Quartz MEMS sensors are limited by either the miniaturization process and the monolithic integration of this material on silicon. These bottlenecks were overcome with the first on-chip chemical integration and nanostructuration of piezoelectric quartz MEMS resonators in the form of high-quality cantilevers.

1.1.1. INTERVIEW: Named talent says the statement above in an interview-style shot, looking slightly off-camera.

1.2. **Adrian Carretero:** From a technological perspective, these novel quartz-based devices open the door to the development of active MEMS engineered from lead-free ferroelectric oxide materials, providing high force and mass sensitivity while preserving the mechanical quality factor.

1.2.1. INTERVIEW: Named talent says the statement above in an interview-style shot, looking slightly off-camera.

Protocol

2. Preparation of PDMS templates and gel film deposition on SOI substrates by dip-coating

2.1. Begin by mixing 1 part of the curing agent with 10 parts of elastomer in a beaker on the balance **[1]**. Stir this mixture with a glass stick until a homogenous distribution of air bubbles is obtained **[2]**, then fill the master with PDMS and remove the bubbles in a vacuum chamber **[3]**. Introduce the PDMS and silicon master into a stove at 70°C for 2h **[4]**. Replicate the silicon master using the PDMS solution as described in the manuscript **[5]**.

2.1.1. Talent mixing the chemicals

2.1.2. Talent stirring the mixture with glass stick

2.1.3. Talent fill the silicon master with PDMS and removing air bubbles in vacuum chamber.

2.1.4. Talent introduce PDMS and silicon master into a stove.

2.1.5. Talent separating the silicon master and the PDMS template.

2.2. Prepare 2 by 6-centimeter-sized substrates by cutting a 2-inch p-type SOI wafer in a direction parallel or perpendicular to the wafer flat using a diamond tip, ensuring that the conductivity of the silicon device layer is between 1 and 10 ohms per centimeter **[1-TXT]**.

2.2.1. Talent cutting the SOI wafer to prepare substrates. **TEXT: SOI: Silicon-On-Insulator**

2.3. To eliminate possible fabrication polymers, introduce these substrates into a piranha solution for 20 minutes **[1]**.

2.3.1. Talent placing substrates in piranha solution.

2.4. Hang the prepared SOI substrate from the dip-coater arm **[1]**, place a beaker underneath it and fill it with Sr based solution **[2]**. In order to obtain a homogenous silica film, set the dip-coater's chamber to 40% relative humidity and 25 degrees Celsius **[3]**. *Videographer: This step is important!*

2.4.1. Talent hanging the SOI substrate.

2.4.2. Changed shot : Talent placing the beaker under the SOI substrate and fill it with Sr based solution.

2.4.3. LAB MEDIA: Screenshot 1.PNG

2.5. Adjust the dip coating sequence to a speed of 300 millimeters per minute at the immersion and withdrawal and start dip process at 40% of relative humidity **[1]**. *Videographer: This step is important!*

2.5.1. Talent starting the dip-coating process. NOTE: Slated as 2.4.4, take 2 in the video.

2.6. After dip-coating, introduce the SOI substrate into a furnace at 450 degrees Celsius for 5 minutes to consolidate the gel film to a thickness 200 nanometers **[1]**. Repeat the dip-coating twice to produce a film with approximately 600-nanometer thickness **[2]**.

2.6.1. Talent introducing the SOI substrate in furnace

2.6.2. Talent repeating the process to obtain the desired thickness of film.

3. Surface micro/nanostructuration by soft imprint lithography and gel film crystallization by thermal treatment

3.1. Start a new dip-coating and place the prepared PDMS mold on the SOI substrate **[1]**. Put the apparatus in the furnace at 70 degrees Celsius for 1 minute **[2]** and then at 140 degrees Celsius for 2 minutes **[3]**. *Videographer: This step is important!*

3.1.1. Talent placing the PDMS mold on the SOI substrate NOTE: Slated as 3.1.2, take 2 in the video.

3.1.2. Talent placing the set apparatus in furnace at 70°C NOTE: Slated as 3.1.2, take 1 in the video.

3.1.3. Added shot: Talent placing the set apparatus in furnace at 140°C

~~3.1.4. Talent allowing the apparatus to cool~~

3.2. Remove the PDMS mold to obtain a micro or nanostructured gel film on the SOI substrate **[1]** and then place the SOI substrate in the furnace at 450 degrees Celsius for 5 minutes to consolidate the gel film height to 600 nanometers **[2]**.

3.2.1. Talent removing the PDMS mold

3.2.2. Talent placing the SOI substrate in the furnace.

3.3. Place the sample in a ceramic boat and introduce it into the furnace at 1000 degrees Celsius for 5 hours. Avoid covering the tubular working tube during the thermal treatment in order to saturate the furnace with air. When finished, allow the furnace to cool to room temperature without any programmed ramp **[1]**.

3.3.1. Changed Shot: Talent introducing the sample in furnace on ceramic boat.

4. Preparing and patterning of the quartz samples for the cantilever microfabrication process

4.1. For patterning a cantilever shape on the quartz thin film, begin by putting the samples inside the piranha solution to clean all organic residues **[1]**, then place them on a hot plate at 140 degrees Celsius for 10 minutes of dehumidification **[2]**. *Videographer: This step is important!*

4.1.1. Talent putting the samples inside the solution

4.1.2. Talent placing the sample on hot plate

4.2. Spin AZ2070 negative photoresist at a speed of 4000 rotations per minute for 30 seconds **[1]**, then put the sample on the hot plate to soft bake it at 115 degree Celsius for 60 seconds **[2]**.

4.2.1. Talent spinning the photoresist

4.2.2. Talent putting the sample on hot plate

4.3. Expose the sample to an ultraviolet dose of 37.5 millijoules per square centimeter for 5 seconds **[1]** and put the sample on the hot plate again for a post exposure bake **[2]**.

4.3.1. Talent exposing the sample to ultraviolet doses

4.3.2. Talent placing the sample on hot plate

4.4. Develop the sample in Metal ion free 726 developer for 100 seconds at ambient temperature **[1]**. Rinse it with deionized water **[2]** and dry with nitrogen. Expect a thickness of 5.5 micrometers **[3]**

4.4.1. Talent developing the sample in MIF 726 developer

4.4.2. Talent rinsing the sample with DI water

4.4.3. Talent drying the sample with nitrogen

4.5. Put the sample on the hot plate at 125 degrees Celsius for 10 minutes to hard bake the photoresist **[1]**. Using a reactive ion etching system **[2]** etch the quartz to the silicon layer with the gas flow rate and radiofrequency power settings described in the text manuscript **[3]**. Clean it with plasma at a flow rate of 90 standard cubic centimeters per minute of oxygen for 5 minutes **[4]**.

4.5.1. Talent putting the sample on hot plate

4.5.2. Added shot : Talent putting the sample into reactive ion etching (RIE)

4.5.3. LAB MEDIA: screenshot 2.png *Video Editor: Emphasize the 60 sccm CHF3, 20 sccm 02 and 10 sccm Ar flow rate settings (rows 1 – 3) and the 100W RF power setting (row 13).*

4.5.4. Added shot: Talent taking the sample out

4.6. For realization of the bottom and top electrode, spin AZ2020 negative photoresist **[1]** and perform a soft bake as previously described **[2]**.

4.6.1. Added shot : Talent spinning the photoresist

4.6.2. Talent taking the sample off of hot plate

4.7. Expose the sample to an ultraviolet dose of 23.25 millijoules per square centimeter for 3 seconds **[1]** and put it on the hot plate for a post exposure bake **[2]**.

4.7.1. Talent exposing the sample to ultraviolet doses.

4.7.2. Talent placing the sample on hot plate.

4.8. Develop, rinse, and blow dry the sample as described in the text manuscript. Expect a thickness of 1.7 micrometers **[1]**.

4.8.1. Finished sample.

4.9. Deposit 50 nanometers of Chromium metal and 120 nanometers of Platinum metal at a rate of 4 ampere per second and 2.5 ampere per second, respectively, with electron beam evaporation at 10^{-6} millibars **[1-3]**. Leave the samples in acetone first **[4]** and then in isopropyl alcohol until metal lift-off is successful **[5]**.

4.9.1. Added shot: Talent putting the sample into the evaporation machine

4.9.2. LAB MEDIA: screenshot 3.png

4.9.3. Added shot: Talent taking the sample out. NOTE : [1] describes all these three steps : 4.9.1, 4.9.2, 4.9.3

4.9.4. Talent placing the sample in acetone

4.9.5. Talent placing the sample in Isopropyl alcohol (IPA)

4.10. For patterning the sample to etch the Silicon-100 layer, spin AZ2070 negative photoresist at a speed of 2000 rotations per minutes for 30 seconds **[1]** and put the sample on the hotplate for a soft bake at 115 degree Celsius for 60 seconds **[2]**.

4.10.1. Talent spinning the photoresist

4.10.2. Talent putting the sample on hot plate

4.11. Expose the sample to an ultraviolet dose of 37.5 millijoule per square centimeter for 5 seconds **[1]** and put the sample on the hot plate again for a post exposure bake **[2]**.

4.11.1. Talent exposing the sample to ultraviolet doses.

4.11.2. Talent placing the sample on hot plate.

4.12. Develop, rinse, and dry the sample as described in the text manuscript. Expect a thickness of 5.9 micrometers **[1]**.

4.12.1. Talent drying the sample with nitrogen.

4.13. Put the sample on a hot plate at 125 degrees Celsius for 10 minutes to hard bake the photoresist **[1]**. Using a reactive ion etching system **[2]** etch the silicon layer to the silicon dioxide layer with gas flow rate and radiofrequency power settings described in the text manuscript **[3]**.

4.13.1. Talent putting the sample on hot plate

4.13.2. Added shot: Talent putting the sample into RIE

4.13.3. LAB MEDIA: screenshot 4.png *Video Editor: Emphasize the 60 sccm CHF3, 20 sccm 02 and 10 sccm Ar flow rate settings (rows 1 – 3) and the 100W RF power setting (row 13).*

4.14. To release the cantilever by wet chemical etching, spin AZ2020 negative photoresist at a speed of 2000 rotations per minutes for 30 seconds **[1]** and put the sample on the hotplate for a soft bake at 115 degrees Celsius for 60 seconds **[2]**

4.14.1. Talent spinning the photoresist

4.14.2. Talent putting the sample on hot plate

4.15. Expose the sample to an ultraviolet dose of 37.5 millijoules per square centimeter for 5 seconds **[1]** and put the sample on the hot plate again for a post exposure bake **[2]**.

4.15.1. Talent exposing the sample to ultraviolet doses.

4.15.2. Talent placing the sample on hot plate.

4.16. Develop, rinse, and dry the sample as described in the text manuscript. Expect a thickness of 2.3 micrometers **[1]**.

4.16.1. Finished sample.

4.17. Put the sample on the hot plate at 125 degrees Celsius for 10 minutes to hard bake the resist **[1]**. Put buffered oxide etch solution in a polytetrafluoroethylene-based container and leave the sample in the solution at ambient temperature until all silicon oxide layers are etched under the cantilever **[2]**. Clean the sample carefully with water and remove the resin with acetone and IPA **[3]**. *Videographer: This step is difficult and important!*

4.17.1. Talent putting the sample on hot plate

4.17.2. Talent putting BOE solution in PTFE container

4.17.3. Talent cleaning sample with water, acetone and IPA.

Results

5. Qualitative analysis of the progressive epitaxial nanostructured α-Quartz Film thickness developed on Silicon

5.1. The synthesis and nanostructuration steps of quartz films **[1]** and microfabrication of quartz cantilever were depicted schematically by monitoring different steps with real images **[2]**.

5.1.1. LAB MEDIA: Figure 1 a – e.

5.1.2. LAB MEDIA: Figure 1 f – i.

5.2. The aspects of a nanostructured quartz-based chip with different cantilever dimensions and its cross-sectional image on the SOI substrate are shown here **[1]**

5.2.1. LAB MEDIA: Figure 2a, 2b and 2c

5.3. 2D Micro X-ray diffraction controlled the crystallinity of the different stacking layers of the cantilever. Their thicknesses are indicated in the diffractogram **[1]**.

5.3.1. LAB MEDIA: Figure 2d.

5.4. The detailed crystallization of quartz pillars was analyzed using the electron diffraction technique and FEG-SEM images in the backscattered electrons mode **[1]**.

5.4.1. LAB MEDIA: Figure 2e and f.

5.5. A deeper structural characterization of a single quartz-based piezoelectric nanostructured cantilever was performed by recording the pole figure and rocking curve **[1]**.

5.5.1. LAB MEDIA: Figure 2g – i.

5.6. The Electromechanical response of the quartz-based piezoelectric cantilevers was detected using a Laser Doppler Vibrometer and with an atomic force microscope **[1]**.

5.6.1. LAB MEDIA: Figure 2j.

5.7. The linear dependence of the cantilever amplitude and applied AC voltage was recorded with the optical beam deflection system of the atomic force microscope **[1]**.

5.7.1. LAB MEDIA: Figure 2k and 2l.

Conclusion

6. Conclusion Interview Statements

6.1. **Claire Jolly:** To ensure the preservation of the crystal quality, functionality, and the mechanical quality factor of quartz cantilevers it is necessary to protect the lateral edges of the quartz layer during the release process of the cantilever, to use a buffer HF solution for a gentle release of quartz based chips, and to increase the thickness of the negative resist to permit longer wet etch times.

6.1.1. INTERVIEW: Named talent says the statement above in an interview-style shot, looking slightly off-camera.

6.2. **David Sánchez Fuentes:** This procedure offers major advantages over quartz bulk in terms of size, power consumption and integration cost with CMOS-compatible processes. It could facilitate the future fabrication of single chip solutions for multifrequency devices while preserving miniaturization and cost-effective processes.

6.2.1. INTERVIEW: Named talent says the statement above in an interview-style shot, looking slightly off-camera.