Video Article

Theoretical Calculation and Experimental Verification for Dislocation Reduction in Germanium Epitaxial Layers with Semicylindrical Voids on Silicon

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Abstract

Reduction of threading dislocation density (TDD) in epitaxial germanium (Ge) on silicon (Si) has been one of the most important challenges for the realization of monolithically integrated photonics circuits. The present paper describes methods of theoretical calculation and experimental verification of a novel model for the reduction of TDD. The method of theoretical calculation describes the bending of threading dislocations (TDs) based on the interaction of TDs and non-planar growth surfaces of selective epitaxial growth (SEG) in terms of dislocation image force. The calculation reveals that the presence of voids on SiO_2 masks help to reduce TDD. Experimental verification is described by germanium (Ge) SEG, using an ultra-high vacuum chemical vapor deposition method and TD observations of the grown Ge via etching and cross-sectional transmission electron microscope (TEM). It is strongly suggested that the TDD reduction would be due to the presence of semicylindrical voids over the SiO_2 SEG masks and growth temperature. For experimental verification, epitaxial Ge layers with semicylindrical voids are formed as the result of SEG of Ge layers and their coalescence. The experimentally obtained TDDs reproduce the calculated TDDs based on the theoretical model. Cross-sectional TEM observations reveal that both the termination and generation of TDs occur at semicylindrical voids. Plan-view TEM observations reveal a unique behavior of TDs in Ge with semicylindrical voids (i.e., TDs are bent to be parallel to the SEG masks and the Si substrate).

Introduction

Epitaxial Ge on Si has attracted substantial interests as an active photonic device platform since Ge can detect/emit light in the optical communication range (1.3-1.6 μm) and is compatible with Si CMOS (complementary metal oxide semiconductor) processing techniques. However, since the lattice mismatch between Ge and Si is as large as 4.2%, threading dislocations (TDs) are formed in Ge epitaxial layers on Si at a density of ~10^9/cm^2. The performances of Ge photonic devices are deteriorated by TDs because TDs works as carrier generation centers in Ge photodetectors (PDs) and modulators (MODs), and as carrier recombination centers in laser diodes (LDs). In turn, they would increase reverse leakage current (J_{leak}) in PDs and MODs[1,2,3], and threshold current (J_{th}) in LDs[4,5,6].

Various attempts have been reported to reduce TD density (TDD) in Ge on Si (**Supplemental Figure 1**). Thermal annealing stimulates movement of TDs leading to the reduction of TDD, typically to 2 x 10^7/cm^2. The drawback is the possible intermixing of Si and Ge and out-diffusion of dopants in Ge such as phosphorus[7,8,9] (**Supplemental Figure 1a**). The SiGe graded buffer layer[10,11,12] increases the critical thicknesses and suppresses the generation of TDs leading to the reduction of TDD, typically to 2 x 10^6/cm^2. The drawback here is that the thick buffer reduces light coupling efficiency between Ge devices and Si waveguides underneath (**Supplemental Figure 1b**). Aspect ratio trapping (ART)[13,14,15] is a selective epitaxial growth (SEG) method and reduces TDs by trapping TDs at the sidewalls of thick SiO_2 trenches, typically to <1 x 10^6/cm^2. The ART method uses a thick SiO_2 mask to reduce TDD in Ge over the SiO_2 masks, which locates far above Si and have the same drawback (**Supplemental Figure 1b**,**1c**). Ge growth on Si pillar seeds and annealing[16,17,18] are similar to the ART method, enabling TD trapping by the high aspect ratio Ge growth, to <1 x 10^5/cm^2. However, high temperature annealing for Ge coalescence has the same drawbacks in **Supplemental Figure 1a-c** (**Supplemental Figure 1d**).

To achieve low-TDD Ge epitaxial growth on Si that is free from the drawbacks of the above-mentioned methods, we have proposed coalescence-induced TDD reduction[19,20] based on the following two key observations reported so far in SEG Ge growth[7,15,21,22,23]: 1) TDs are bent to be normal to the growth surfaces (observed by the cross-sectional transmission electron microscope (TEM)), and 2) coalescence of SEG Ge layers results in the formation of semicylindrical voids over the SiO_2 masks.

We have assumed that the TDs are bent owing to the image force from the growth surface. In the case of Ge on Si, the image force generates 1.38 GPa and 1.86 GPa shear stresses for screw dislocations and edge dislocations at distances 1 nm away from the free surfaces, respectively[19]. The calculated shear stresses are significantly larger than the Peierls stress of 0.5 GPa reported for 60° dislocations in Ge[24]. The calculation predicts TDD reduction in Ge SEG layers on a quantitative basis and is in good agreement with the SEG Ge growth[19]. TEM

observations of TDs are carried out to understand TD behaviors in the presented SEG Ge growth on Si[20]. The image-force-induced TDD reduction is free from any thermal annealing or thick buffer layers, and thus is more suitable for photonic device application.

In this article, we describe specific methods for the theoretical calculation and experimental verification employed in the proposing TDD reduction method.

Protocol

1. Theoretical calculation procedure

1. Calculate trajectories of TDs. In the calculation, assume the SEG masks to be thin enough to ignore the ART effect on TDD reduction.
    1. Determine growth surfaces and express them by equation(s). For instance, express the time evolution of a round-shaped cross-section of a SEG Ge layer with the time evolution parameter $n = i$, SEG Ge heights (h_i) and SEG Ge radii (r_i), as shown in the **Supplemental Video 1a** and Eq. (1):
    $$x^2 + \{y - (r_i - h_i)\}^2 = r_i^2 . \quad (1)$$
    2. Determine normal directions for an arbitrary location on the growth surfaces. For the round-shaped cross-section SEG Ge, describe the normal line at (x_i, y_i) as $y = \frac{y_i - (h_i - r_i)}{x_i} x + h_i - r_i$, shown in **Supplemental Video 1b** as a red line. Then, obtain the edge of the TD (x_{i+1}, y_{i+1}) from the point (x_i, y_i) by solving the following simultaneous equations:
    $$\begin{cases} x^2 + \{y - (r_{i+1} - h_{i+1})\}^2 = r_{i+1}^2 & (2a) \\ y = \frac{y_i - (h_i - r_i)}{x_i} x + h_i - r_i & (2b) \end{cases}$$
    3. Calculate a trajectory of one TD depending on the location of TD generation (x_0, 0), as shown in **Supplemental Video 1c**. In other words, a trajectory for an arbitrary TD can be calculated by the method described above.
    4. Calculate TDD assuming that TDs penetrate to the bottom surface and contribute to the reduction of TDD (i.e., TDs below the point where SEG Ge layers coalesce are trapped by semicylindrical voids and never appear on the top surface).

2. Experimental verification procedure

1. SEG mask preparation
    1. Prior to the fabrication of SEG masks, define Ge growth areas by preparing a design file. Inthe present work, prepare line-and-space patterns aligned to the [110] direction and square-shaped Si window areas of 4 mm in width using commercial software (e.g., AutoCAD).
    2. Determine the design of SEG masks(in particular W_{window} and W_{mask})using the software.W_{window} is the window width (Si seed width) and W_{mask} is the SiO_2 mask width, such that SEG Ge layers can coalesce with their adjacent ones. Determine W_{window} and W_{mask} by drawing rectangles by clicking **open file** → **structure** → **rectangle or polyline**.
    NOTE: The width of the rectangles becomes W_{window}, and the interval of the rectangles becomes W_{mask}. In the present work, the minimum values of W_{window} and W_{mask} are 0.5 μm and 0.3 μm, respectively, which are restricted by the resolution in the employed EB lithography system.
    3. As references, draw square-shaped Si window areas of 4 mm in width D, regarded as the blanket areas. Click **open file** → **structure** → **rectangle or polyline** to draw the square-shaped Si window. Use the schematics shown in **Figure 1** to prepare the line-and-space patterns and the 4 mm square blanket area.
    4. Prepare B-doped p-Si (001) substrates with the resistivity of 1-100 Ω·cm. In the present work, use 4-inch Si substrates. Clean the substrate surfaces with Piranha solution (a mixture of 20 mL of 30% H_2O_2 and 80 mL of 96% H_2SO_4) as necessary.
    5. Open the lid on a tube furnace and load the Si substrates into the furnace using a glass rod. In the present work, oxidize 10 Si substrates at one time.
    6. Start to blow dry N_2 gas into the furnace by opening the gas valve. Then, set the gas flow rate to 0.5 L/m by controlling the valve.
    7. Set the annealing temperature by changing the program. In the present work, use "pattern step (mode 2)" and set the process temperature to 900 °C. Then, run the program by pushing **function** → **run**.
    8. As the temperature reaches 900 °C, close the dry N_2 valve, open the dry O_2 valve (O_2 flow = 1 L/m), and keep for 2 h.
    NOTE: Perform steps 2.1.9-2.1.16 in a yellow room.
    9. Coat the oxidized Si substrates with a surfactant (OAP) using a spin coater and then bake at 110 °C for 90 s on a hotplate.
    10. After the surfactant coating, coat the Si substrates with a photoresist (e.g., ZEP520A) using a spin coater and then bake at 180 °C for 5 min on a hotplate.
    11. Load the Si substrates with the surfactant and photoresist into an electron beam (EB) writer.
    12. Read the design file (prepared in step 2.1.2) in the EB writer and make an operation file (WEC file). Set dose quantity as 120 μC/cm^2 in the WEC file. As the substrate loading finishes, perform EB exposure by clicking the **single exposure** button.
    13. Unload the substrate from the EB writer by clicking **wafer carry** → **unload** as the exposure finishes.
    14. Prepare a photoresist developer (ZED) and a rinse for the developer (ZMD) in a draft chamber. Dip the exposed Si substrates into the developer for 60 s at room temperature.
    15. Remove the Si substrates from the developer, and then dry the substrate with N_2 gas.
    16. Put the developed Si substrates on a hotplate to bake at 110 °C for 90 s.
    17. Dip the Si substrates into a buffered hydrofluoric acid (BHF-63SE) for 1 min in order to remove part of the SiO_2 layers exposed to the air as the result of EB exposure and development.
    18. Remove the photoresist from the Si substrates by dipping into an organic photoresist remover (e.g., Hakuri-104) for 15 min.

19. Dip the Si substrates into 0.5% diluted hydrofluoric acid for 4 min to remove the thin native oxide in the window regions but to retain the SiO_2 masks. Then load onto an ultrahigh-vacuum chemical vapor deposition (UHV-CVD) chamber to grow Ge. **Figure 2** shows the UHV-CVD system used in the present work.

2. Epitaxial Ge growth
    1. Load the Si substrate with SEG masks (fabricated as in step 2.1) into a load lock chamber.
    2. Set the buffer/main growth temperature in the **Recipe** tab shown on the operation computer. Determine the durations for the main growth of Ge so that SEG Ge layers coalesce with adjacent ones. To decide the durations for the main growth, consider the growth rate of Ge on the {113} planes, which determines the growth in the in-plane/lateral direction[26]. In the present work, set the durations for the main growth as 270 min and 150 min for 650 °C and 700 °C, respectively.
    3. Click **start** in main window, and then the Si substrate is automatically transferred into the growth chamber.
    NOTE: Protocol on epitaxial Ge growth (steps 2.2.4-2.2.7) is automatically processed.
    4. Grow Ge buffer on the loaded Si substrate at low-temperature (≈380 °C). Use GeH_4 diluted at 9% in Ar as the source gas and keep the partial pressure of GeH_4 for 0.5 Pa during the buffer growth.
    5. Grow Ge main layer at an elevated temperature. Keep the partial pressure of GeH_4 for 0.8 Pa during the main growth. In the present work, use two different temperatures of 650 and 700 °C for the main growth temperature in order to compare SEG Ge with a round-shaped cross-section and with a {113}-facetted cross-section[25].
    NOTE: The growth rate of Ge on the (001) plane was 11.7 nm/min independent of the temperature.
    6. In order to visualize the evolution of SEG Ge and their coalescence, perform Ge growth with periodic insertion of 10-nm-thick $Si_{0.3}Ge_{0.7}$ demarcation layers on another Si substrate. $Si_{0.3}Ge_{0.7}$ layers were formed using Si_2H_6 and GeH_4 gases. During the $Si_{0.3}Ge_{0.7}$-layer growth, set the partial pressure of Si_2H_6 gas at 0.02 Pa and the partial pressure of GeH_4 gas at 0.8 Pa.
    7. As the Si substrate is automatically transferred from the growth chamber to the load lock chamber, vent the load lock chamber and unload the Si substrate manually.

3. Etch pit density (EPD) measurements
    1. Dissolve 32 mg of I_2 in 67 mL of CH_3COOH using an ultrasonic cleaning machine.
    2. Mix the I_2-dissolved CH_3COOH, 20 mL of HNO_3, and 10 mL of HF.
    3. Dip the Ge-grown Si substrates into the $CH_3COOH/HNO_3/HF/I_2$ solution for 5-7 s in order to form etched pits.
    4. Observe the etched Ge surfaces with an optical microscope (typically 100x) to ensure that etched pits are successfully formed.
    5. Employ an atomic force microscope (AFM) to count the etched pits. Put the etched Ge sample on an AFM stage, and then approach the probe by clicking auto **approach**.
    6. Decide the observation area using an optical microscope integrated with an AFM, and scan five different 10 µm x 10 µm areas. The amplitude damping factor is automatically determined.

4. TEM observations
    1. Pick up TEM specimens from the coalesced/blanket Ge layers by using a focused Ge ion beam (FIB micro sampling method)[27].
    2. Polish the TEM specimens in an ion milling system using Ar ions. In the present work, thin down TEM specimens for cross-sectional observations to be 150-500 nm in the [110] direction, and for plan-view observations to be 200 nm in the [001] direction.
    3. For plan-view TEM specimens, protect the top surfaces of the Ge layers with amorphous layers, and then thin down from the bottom (substrate) side of the Ge layers.
    4. Perform TEM observations under an acceleration voltage of 200 kV. Perform cross-sectional bright-field scanning TEM (STEM) observations in order to observe thick (500 nm) TEM specimens.
    5. For a coalesced Ge with $Si_{0.3}Ge_{0.7}$ demarcation layers, perform cross-sectional high-angle annular dark field (HAADF) STEM observations under an acceleration voltage of 200 kV.

Representative Results

Theoretical Calculation

Figure 3 shows calculated trajectories of TDs in 6 types of coalesced Ge layers: here, we define the aperture ratio (APR) to be $W_{window}/(W_{window} + W_{mask})$. **Figure 3a** shows a round-shaped SEG origin coalesced Ge of APR = 0.8. Here, 2/6 TDs are trapped. **Figure 3b** shows a {113}-facetted SEG origin coalesced Ge of APR =0.8. Here, 0/6 TDs are trapped. **Figure 3c** shows a round-shaped SEG origin coalesced Ge of APR = 0.1. Here, 5/6 TDs are trapped. **Figure 3d** shows a {113}-facetted SEG origin coalesced Ge of APR = 0.1. Here, 6/6 TDs are trapped. **Figure 3e** shows a round-shaped SEG origin coalesced Ge of APR = 0.1, in case that Ge grows on SiO_2 masks. Here, 0/6 TDs are trapped. **Figure 3f** shows a {113}-facetted SEG origin coalesced Ge of APR = 0.1, in case that Ge grows on SiO_2 masks. Here, 0/6 TDs are trapped.

The trajectories of 6 TDs generated at (x_0, 0), where x_0 = 0.04, 0.1, 0.2, 0.4, 0.6, and 0.8 times $W_{window}/2$, are shown as red lines in each figure. TDs located above the coalescence points of these two SEG Ge layers propagate upward to the top surface, while TDs below the points propagate downward to remain at the void surface over the SiO_2 mask.

In **Figure 3a-3d**, it is assumed that SEG Ge does not grow on SiO_2. Thus, the sidewalls of the {113}-facetted SEG Ge are assumed to be round-shaped in order to not touch the SiO_2 masked area. It is clearly shown that round-shaped SEG and then coalesced Ge are more effective to reduce TDD at an APR of 0.8, than the {113}-facetted case, while {113}-facetted and then coalesced Ge are more effective than a round-shaped one at an APR of 0.1. This "crossing" is ascribed to the presence of {113} facets near the SEG top: {113} facets are more deviated from the [001] direction than round-shaped surfaces.

Figure 3e and **Figure 3f** show coalesced Ge at an aperture ratio of 0.1, assuming that Ge is not nucleated on SiO_2 but shows wetting with the SiO_2 mask, widely reported in previously reported Ge coalescence[13,15,22,28,29,30,31]. As shown in **Figure 3e** and **Figure 3f**, there is no semi cylindrical void between two SEG and thus no TD is trapped at the surface.

Figure 4\ shows calculated TDDs in coalesced Ge. In **Figure 4**, the red line shows calculated TDDs in coalesced Ge originating from the round-shaped SEG Ge, and the blue line shows calculated TDDs in coalesced Ge originating from the {113}-facetted SEG Ge. Since TDs in Ge on Si originate from the lattice mismatch between Ge and Si, it is assumed that TD generation occurs only at interfaces between Ge and Si. In other words, TDD should be reduced with APR.

When APR is larger than 0.11, the round-shaped SEG Ge is more effective than the {113}-facetted one (**Figure 3a** and **Figure 3b**). When APR is smaller than 0.11, on the other hand, the {113}-facetted SEG Ge becomes more effective than the round-shaped one (**Figure 3c** and **Figure 3d**). As in **Figure 3**, such crossing is ascribed to the presence of {113} facets near the SEG top ($x_0 \approx 0$). Note that **Figure 3e** and **Figure 3f** correspond to the black line in **Figure 4**, showing the reduction of TDD from the reduction of APR, but not to the coalescence (i.e., SEG Ge wetting with SiO_2 has a negative effect against the TDD reduction).

Experimental Verification

Figure 5 show typical cross-sectional scanning electron microscopy (SEM) images (**Figure 5b-5d, 5f**) and the distribution maps (**Figure 5a**, 5e) showing whether coalescence occurs or not. **Figure 5b-5d**, **5f** show cross-sectional SEM images of non-coalesced SEG Ge layers (**Figure 5b**, grown at 700 °C; **Figure 5f**, grown at 650 °C), coalesced SEG Ge layers with a non-flat top surface (**Figure 5c**, grown at 700 °C), and coalesced SEG Ge layers with a flat top surface (**Figure 5d**; grown at 700 °C). SEM images shown in **Figure 5b** and **Figure 5d** are polished by a focused ion beam after deposition of Pt protection layers. The coalescence occurs when the W_{window} and W_{mask} are smaller than 1 µm for the present growth conditions. The SEG masks with W_{mask} of 1 µm or larger prevent the coalescence of Ge due to the small amount of Ge growth in the lateral direction[26]. The SEG masks with a W_{window} of 2 µm or greater also prevent the coalescence of Ge, although the coalescence took place when the W_{window} is smaller than 1 µm. This is because the lateral growth rate of Ge over SiO_2 depends on the W_{window}[30]. The mask and window pattern dependence are summarized in **Figure 7a** (700 °C) and **Figure 7e** (650 °C).

Comparing the non-coalesced SEG Ge layers (**Figure 4b** and **Figure 4f**), it is clearly shown that the SEG Ge layer grown at 700 °C has a round-shaped cross-section while the SEG Ge layer grown at 650 °C has a {113}-facetted cross-section. As in **Figure 5b**, the growth at 700 °C shows a round-shaped SEG Ge without Ge growth on SiO_2 (i.e., no wetting with the SiO_2 mask). Therefore, the growth proceeds like **Figure 3a** and **Figure 3c**. On the other hand, as in **Figure 5f,** an {113}-facetted SEG Ge appears at 650 °C. It is strongly suggestive that the Ge would show wetting with the SiO_2 mask. In contrast, the edge is round-shaped (i.e., not wetting). Therefore, the growth at 650 °C is in between **Figure 3b** (no wetting) and **Figure 3f** (perfect wetting). This indicates that the TDD reduction should be in between **Figure 3b** and **Figure 3f**. Considering the theoretical results shown in **Figure 6**, these differences in the SEG Ge cross-sections should strongly influence TDDs in the coalesced Ge layers.

The difference in wetting growth on SiO_2 can be understood as follows. The contact angle between Ge and SiO_2 (θ) is determined by Young's equation:

$$\gamma_{SiO2} = \gamma_{Ge} \cos\theta + \gamma_{int} \qquad (4)$$

Here, γ_{SiO2}, γ_{Ge}, and γ_{int} are SiO_2 surface free energy, Ge surface free energy, and Ge/SiO_2 interfacial free energy, respectively. The angle of the SEG Ge sidewall becomes larger as Ge growth proceeds. When the angle of the SEG Ge sidewall reaches the contact angle θ, the SEG Ge needs to grow in the vertical ([001]) or lateral ([]) direction. In the case for 650 °C growth, the vertical growth is severely limited by the {113} facets, and thus SEG Ge prefers to grow in lateral direction (i.e., wetting growth). Even though the wetting could generate dislocations at the Ge and SiO_2 interface, it is finally to be terminated at the semicylindrical void surface. In the case for 700 °C growth, Ge can grow in a vertical direction, and the contact angle is larger than that for 650 °C because of a larger γ_{int}. This would be the reason why 650 °C-grown Ge shows wetting over SiO_2 while 700 °C grown-Ge does not.

For Ge after coalescence, the cross-sectional structure is not influenced by the growth temperature: coalesced Ge layers grown at 650 °C and the ones grown at 700 °C could not be differentiated by cross-sectional SEM observations.

Note that for the fabricated patterns, W_{window} values were larger and W_{mask} values were smaller than the designed ones because an isotropic wet etching process was employed to fabricate the mask. The actual values of W_{window} and W_{mask} were obtained by cross-sectional SEM observations after Ge growth.

In addition to that, the thickness of the mask SiO_2 layers was 30 nm according to the cross-sectional SEM observations and spectroscopic ellipsometry measurements. Such thin SiO_2 layers were employed to examine the TDD reduction explained in **Figure 3** and **Figure 4**, removing the effect of epitaxial necking on the ART. In the present work, the aspect ratios are lower than 0.05, which is small enough to ignore the effect of epitaxial necking on the ART.

Figure 6a shows a cross sectional HAADF STEM for a SEG with $Si_{0.3}Ge_{0.7}$ demarcation layers, and a schematic illustration of **Figure 6a** is shown in **Figure 6b** (W_{window} = 0.66 µm, W_{mask} = 0.84 µm). The $Si_{0.3}Ge_{0.7}$ demarcation layers clearly show the surface shapes during the growth at 700 °C. The STEM image shows the Ge surfaces of each growth step from round-shaped SEG to a flat epitaxial layer formed after the coalescence. The growth rate just after coalescence is strongly enhanced at the coalesced areas. This rapid growth is probably induced by the Ge epilayer, minimizing its surface area to get energetically stabilized.

In contrast to the pure Ge SEG, the presented Ge SEG with the $Si_{0.3}Ge_{0.7}$ demarcation layers show wetting with the SiO_2 masks (**Figure 8a**). The difference in wetting is perhaps due to the insertion of $Si_{0.3}Ge_{0.7}$ demarcation layers, whose nucleation is enhanced on SiO_2 layers unlikely that of Ge.

Flat-top coalesced Ge (blue-circled areas in **Figure 5a** and **Figure 5e**) are used for EPD measurements. The Ge layers were etched on average by 200 nm. Typical AFM images after etching are shown in **Figure 7a** and **Figure 7b**, taken for 1.15-µm-thick coalesced Ge grown at 700 °C (W_{window} = 0.66 µm and W_{mask} = 0.44 µm) and 2.67-µm-thick coalesced Ge grown at 650 °C (W_{window} = 0.66 µm and W_{mask} = 0.34 µm). As a reference, the image of the 1.89-µm-thick blanket Ge grown at 700 °C is shown in **Figure 7c**. The dark dots in the AFM images are etched pits indicating the presence of TDs. The EPD values from **Figure 7a**-7c were obtained to be 7.0 x 10^7/cm^2, 7.9 x 10^7/cm^2, and 8.7 x 10^7/cm^2, respectively. Our previous reports showed that the obtained EPDs in this etching condition are equal to TDDs determined by plan-view transmission electron microscopy (TEM)[4,32,33,34]. The measured EPD of blanket Ge layer (7.9 ± 0.8 x 10^7/cm^2) agrees well with TDD obtained from plan-view TEM observation with a relatively large area of 6 x 8 µm^2 (8.7 ± 0.2 x 10^7/cm^2), indicating that the EPD is equal to TDD.

In order to compare the experimentally obtained TDDs with calculations, take into account the effect of thickness on TDD. There is a trend that TDD decreases as the Ge thickness increases because of increased chances for the pair annihilation of TDs. Therefore, the reduction of TDD observed for the coalesced Ge, thinner than blanket Ge, should be ascribed to the mechanism described in **Figure 3** and **Figure 4** (i.e., we need to calculate the normalized TDD to compare the experimentally obtained TDDs with the calculated ones in **Figure 4**). Before the normalization, a correction of TDD for blanket Ge ($\rho_{blanket}$) was performed, considering the thickness and the growth temperature on TDD. Similar to the previous reports[35,36], $\rho_{blanket}$ [/cm^2] is approximately expressed as 2.52 x 10^{13} x [d (nm)]$^{-1.57}$ for the Ge layers grown in the temperature range of 530-650 °C using a UHV-CVD. Here, d is the thickness of the blanket Ge layer. $\rho_{blanket}$ [/cm^2] is reduced for the Ge layers grown at 700 °C, and approximately expressed as 2.67 x 10^{12} x [d (nm)]$^{-1.37}$.

Figure 7d shows the normalized TDD as a function of APR, $W_{window}/(W_{window} + W_{mask})$. TDDs in coalesced Ge grown at 650 °C are shown as blue triangles and those grown at 700 °C as red diamonds. Since SEG Ge at 650 °C shows some wetting with the SiO_2 mask, the growth data should fall in between the black and blue lines. SEG Ge at 700 °C should be on the red line. The experimental results are in good agreement with the calculation based on the cross-sectional shape and wetting conditions.

As described above, it is concluded that the behavior of TDs is well explained by the model based on the image force of growth surfaces on TDs. In order to understand the interaction of TD with the surface, we have observed TDs with a bright-field cross sectional STEM. A defect is observed being bent and terminated on a surface of a semicylindrical void in **Figure 8a**. This behavior of the TD is quite similar to calculated trajectories of TDs shown in **Figure 3**. However, the observed trajectory of TD does not exactly reproduce the one we predicted in **Figure 3**. The difference would be explained as the result of a TD transformation in order to minimize its energy during or after the growth (e.g., temperature decrease from growth temperature to room temperature). **Figure 8b** shows a simulation of strain in the coalesced Ge epilayer on Si. Tensile strain is induced in the Ge layer on Si because of the mismatch of thermal expansion coefficient between Ge and Si. The simulation indicates that strain accumulation occurs at the top of the semicylindrical voids and strain relaxation at the sub-surface layer of the semicylindrical voids, which would motivate TDs to transform.

On the other hand, **Figure 8c** shows defect generation at the top of a void, although the generation point would be removed during the preparation of the TEM specimen. The defect in **Figure 8c** is close to a straight line, but the angle between the defect and (001) plane (≈78.3°) does not agree with that for the {111} plane (54.7°).

The electron diffraction pattern shown in **Figure 8d** was obtained near the defect in **Figure 8c**. The absence of streak light indicates that there should not be a 2D structure (i.e., the defect is a dislocation). In previous reports[28,29,30,31,37], 2D defects were formed showing clear a streak light in electron diffraction patterns, which is against the one observed in the present work. The observation results (the absence of 2D defects) supports the prediction that the voids and their free surfaces contribute to release strain in Ge on Si, or otherwise cause the crystal misorientations between adjacent SEG Ge layers. This is consistent with a previous report briefly suggesting that the formation of 2D defects is prevented in coalesced SEG Ge layers with voids on the SiO_2 masks[38].

There are two candidates for the TD generation shown in **Figure 10c**: the strain distribution and the misorientation between SEG Ge layers. In epitaxial Ge on Si, the tensile strain is induced in Ge due to the mismatch of thermal expansion coefficient between Ge and Si[39]. The simulation result shown in **Figure 8b** indicates accumulation of tensile-strain (~0.5%) at the top of the void as mentioned above. Such strain accumulation at the void top could result in TD generation shown in **Figure 8c**. Another candidate, the misorientation between SEG Ge layers, has been assumed to generate 2D defects as observed in previous reports showing coalescence of SEG Ge layers[28,29,30,31,37]. In the present work, however, the generation of 2D defects would be suppressed owing to the presence of voids as briefly mentioned in a previous report[38], but result in the TD generation owing to imperfect suppression. More detailed discussion for the misorientation-induced dislocation will be described in a later part with schematic illustrations (**Figure 12**).

Figure 9a and **Figure 9b** show bright-field plan-view TEM images of a coalesced Ge layer (W_{window} = 0.82 µm, W_{mask} = 0.68 µm) and a blanket Ge layer, respectively, grown on the same substrate. For the plan-view TEM observations, TEM specimens were formed using the top 200 nm regions of the Ge layers as described in step 2.4.3 and are indicated by red dashed squares in the schematic cross-sections at the top of **Figure 9**. SiO_2 mask stripes are aligned to the [110] direction for the coalesced Ge in **Figure 9a**. The plan-view TEM image shown in **Figure 9a** was taken for a 6 µm x 8 µm area. Although there are five pairs of SiO_2 masks and Si window areas in this TEM image, the areas above the SiO_2 masks and Si windows are not distinguishable in the TEM image. This is because the observed area (top 200 nm) is far above where semicylindrical voids are located (bottom 150 nm).

It is found that TDDs obtained from **Figure 9a** and **Figure 9b** are 4.8 x 10^7/cm^2 and 8.8 x 10^7/cm^2, respectively. As shown in **Figure 7d**, EPD measurements reveal that TDD in the coalesced Ge layer (W_{window} = 0.82 µm and W_{mask} = 0.68 µm) is 4 x 10^7 cm^{-2}. Thus, the TDD in **Figure 9a** shows a good agreement with the EPD shown in **Figure 7**. It is also notable that neither EPD measurements nor TEM observations show TDD re-increase, which is frequently shown when SEG Ge layers coalesce (i.e., the TDD re-increase owing to generation of TDs (**Figure 8b**) is suppressed to such an extent that the TDD re-increase is ignorable in the present TDD range (on the order of 10^7/cm^2)).

It should be remarked that a TD-free area as large as 4 μm x 4 μm is realized in the coalesced Ge, as in **Figure 9a**. Although the blanket Ge in **Figure 9b** shows TDs with a relatively uniform distribution, the coalesced Ge has high and low TDD areas. Such differences in TD distribution suggest that further TDD reduction would be achievable in the coalesced Ge. 1 TD in a 4 μm x 4 μm area, which is observed in **Figure 9a**, corresponds to TDD of 6.25 x 10^6/cm^2.

Comparing coalesced Ge (**Figure 9a**) and blanket Ge (**Figure 9b**), it is clear that the lengths of the defect lines in coalesced Ge are longer than those in blanket Ge. In coalesced Ge, there are typically 1-μm-long defect lines, and they are aligned to the [110] direction. Note that the [110] direction is the length direction of the SiO_2 stripes. There are two possible explanations for such long defect lines: (i) 2D defects are observed and (ii) dislocations are inclined in the [110] direction. However, 2D defects are immediately denied because of the widths of the observed long defects (i.e., 2D defects on {111} planes should show wider defect lines). Geometrically, 2D defects on the {111} planes should show 140-nm-wide defect lines, taking into account the thickness of the TEM specimen (200 nm) and the angle of the {111} with (001) planes (54.7°). The plan-view TEM image shows that the defect lines are 10-20 nm in width, which is much narrower than 140 nm. Thus, the defects shown as long lines should be ascribed to (ii) dislocations inclined in the [110] direction. A simple geometrical calculation gives the angle between the inclined dislocations and (001) planes: $\tan^{-1}$(200 nm/1 μm) = 11.3°. Note that, as shown in **Figure 8b**, TDs in blanket Ge tend to be directed almost vertical to the substrate if no post-growth annealing is performed, showing small black dots in plan-view TEM images.

For more detailed analysis of the inclined TDs, a small area with high-TDD is arbitrarily observed as in **Figure 10**. The TEM specimen was prepared from the top 200 nm of the coalesced Ge layer, the same as the plan-view TEM observations above.

Figure 10a and **Figure 10b** show dark-field (g = [220] for **Figure 12a** and $[2\bar{2}0]$ for **Figure 12b**) plan-view TEM images taken at the same area. In **Figure 12**, four inclined dislocations were observed in a 4 μm x 4 μm area. **Figure 10b** reveals that one inclined dislocation (the red-circled one) disappears when diffraction vector **g** = $[2\bar{2}0]$, which indicate that the Burgers vector is determined to be [110] or $[1\bar{1}0]$ for the red-circled dislocation. Since the defect line is in the [110] direction, the dislocation is found to be a screw dislocation. The other three inclined dislocations (green-circled ones) are ascribed to the mixed dislocations because they did not disappear whatever diffraction vector **g**

There are two possible explanations for the inclination of TDs in coalesced Ge layers: (i) Ge growth in [110] direction, and (ii) defect generation when SEG Ge layers coalesce.

Ge growth in [110] direction

Figure 11 shows a plan-view SEM image and the growth process to form a flat epitaxial layer from a non-planar SEG surface as a schematic movie. Reflecting the edge undulation of the SiO_2 stripe patterns formed by the EB lithography and wet chemical etching, the coalescence preferentially starts at some points, and then proceeds in the [110] and $[\bar{1}\bar{1}0]$ directions above the SiO_2 masks. **Figure 11b** and **Figure 11c** schematically show the bird's eye view and the $(1\bar{1}0)$ cross-sectional view when SEG Ge layers are partly coalesced. A TD generated at a growth window appears above the void as shown in **Figure 3**, and then the TDs start to propagate in the [110] or $[\bar{1}\bar{1}0]$ direction due to the image force. This leads to TDs inclined in the [110] direction (as in **Figure 9a**). The red solid line in **Figure 11c** shows a TD bent in the [110] direction according to the model above, which explains the presence of the inclined TDs observed in **Figure 9a** and **Figure 10** on a qualitative basis.

The mechanism can explain both edge and screw TDs, taking into account the Burgers vectors of TDs generated at Ge/Si interfaces[40]. As Ge is grown on a Si substrate, edge misfit dislocations (MDs) are formed to release strain, and MDs are aligned in the [110] or $[1\bar{1}0]$ direction. The MDs form threading segments (i.e., TDs), and the Burgers vectors for the TDs originated from MDs aligned in the [110] direction (MD_{110}) are a/2$[1\bar{1}0]$ or a/2$[\bar{1}10]$ (a: the lattice constant). On the other hand, the Burgers vectors are a/2[110] or a/2$[\bar{1}\bar{1}0]$ for the TDs originated from MDs aligned in the $[1\bar{1}0]$ direction ($MD_{1\bar{1}0}$). In the case that the TDs from MD_{110} are inclined to the [110] direction, plan-view TEM observations show the TDs as edge dislocations. Similarly, when the TDs from $MD_{1\bar{1}0}$ are inclined to the [110] direction, they are observed as screw dislocations.

Defect generation when SEG Ge layers coalesce

Figure 12 shows schematics explaining generation of defects when SEG Ge layers coalesce with small rotation (i.e., misorientation). As schematically illustrated in **Figure 12**, the misorientation should generate edge/screw/mixed dislocations at the coalescence interface. In **Figure 12**, misorientation between two SEG Ge layers in the [110] direction is decomposed into three types of rotations. **Figure 12a**-12c shows the rotation around the [110] axis, the [001] axis, and the $[1\bar{1}0]$ axis, respectively.

The coalescence in **Figure 12** is assumed to occur between a strictly epitaxial Ge layer (Ge (001)) and an adjacent SEG Ge layer with a misorientation (m-Ge). The rotation around the [110] axis (**Figure 12a**) results in the generation of edge dislocations parallel to the [110] direction at the boundary indicated as a dashed line. Similarly, as in **Figure 12b**, the edge dislocations parallel to the [001] direction are generated as a result of the rotation around the [001] axis. On the other hand, the rotation around the $[1\bar{1}0]$ axis, shown in **Figure 12c**, generates a screw dislocation network, which is composed by dislocations of ***b*** = [110] and ***b*** = [001], being similar to the case for direct bonding of Si (001) surfaces showing screw dislocation network[41]. The screw TD observed in **Figure 10** could be ascribed to the coalescence with misorientation of a rotation around $[1\bar{1}0]$ axis. The combination of rotations around [110] axis (**Figure 12a**) and around $[1\bar{1}0]$ axis (**Figure 12c**) can explain the mixed TDs shown in **Figure 12**. The mixed dislocation shown in **Figure 9b** is also explained by the combination of the rotation around the [001] axis (**Figure 12b**) and the rotation on the $[1\bar{1}0]$ axis (**Figure 12c**).

Assuming that the dislocations originated from the misorientation are generated at a density of 1 x 10^7/cm^2, the average angle of the rotation around [] axis is estimated to be 0.034° [42]. Compared to the estimation, we have already reported that there are fluctuations of orientation in a line-shaped SEG Ge layer for 100 arcsec (= 0.028°), employing micro-beam X-ray diffraction observations[43]. The reported fluctuations of orientation and estimated rotation angle show good agreement, which supports the TD generation mechanism based on misorientations.

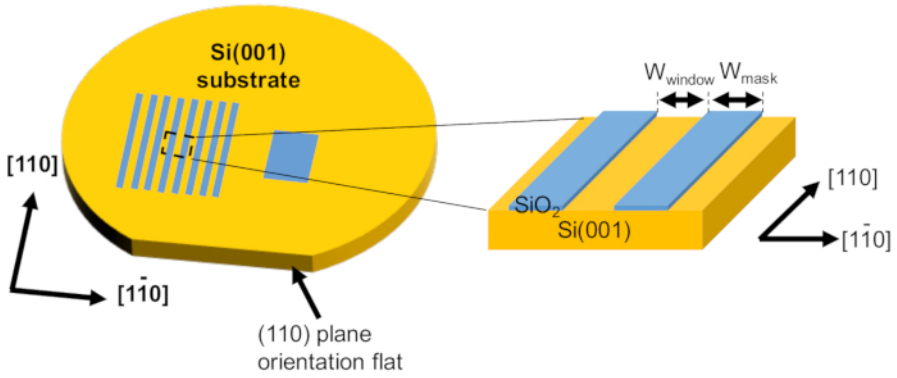

Figure 1: Schematic illustrations of line-and-space shaped and 4 mm square SEG masks on a Si(001) substrate. Please click here to view a larger version of this figure.

Figure 2: Pictures for parts of an UHV-CVD machine; gas cabinet, process chamber, load lock chamber, and operation computer. Please click here to view a larger version of this figure.

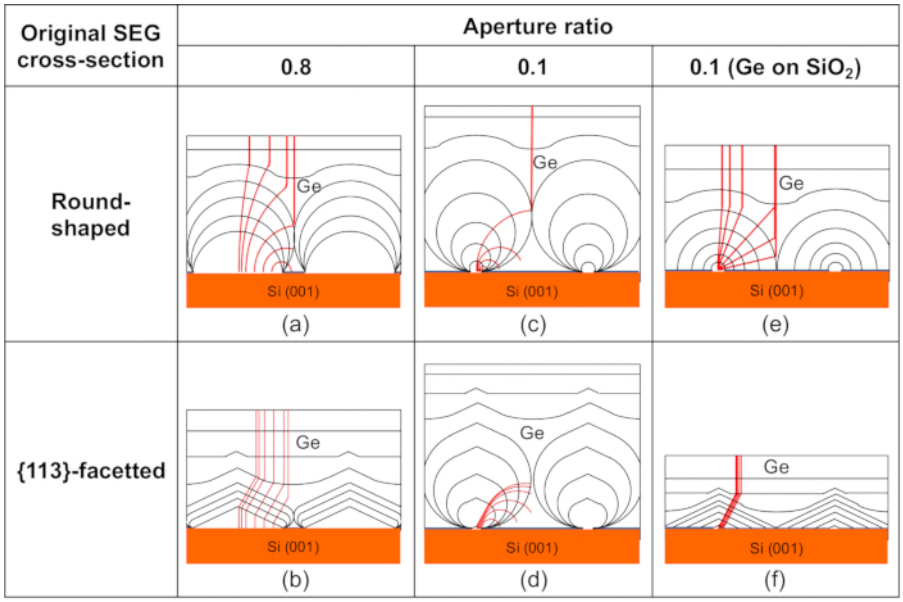

Figure 3: Calculated trajectories of 4 TDs in (a) round-shaped SEG origin, aperture ratio = 0.8, (b) round-shaped SEG origin, aperture ratio = 0.1, (c) {113}-facetted SEG origin, aperture ratio =0.8, and (d) {113}-facetted SEG origin, aperture ratio = 0.1. Please click here to view a larger version of this figure.

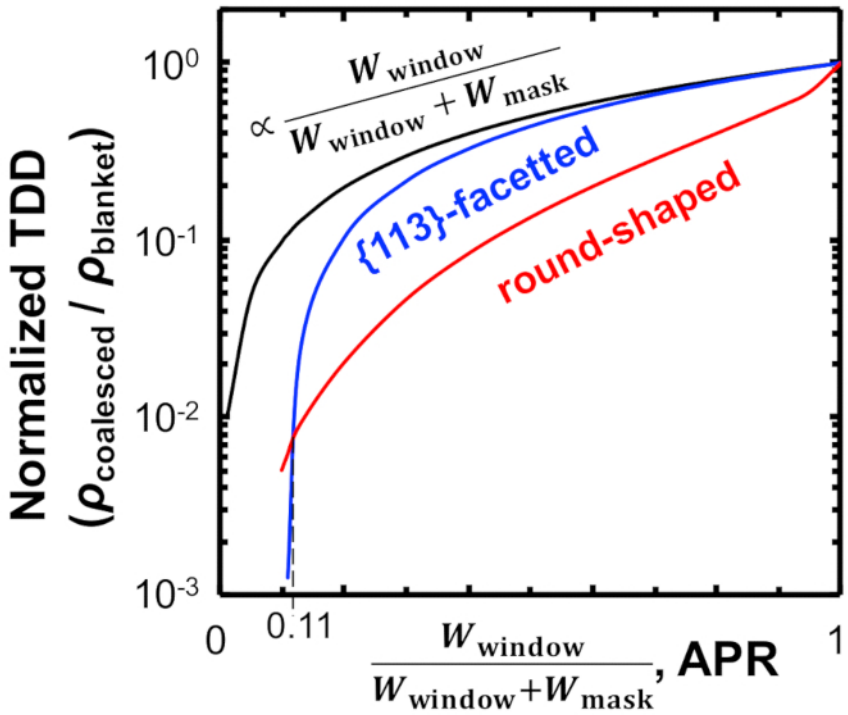

Figure 4: Calculated TDDs in coalesced Ge originated from {113}-facetted SEG Ge (blue line) and round-shaped SEG Ge (red line). Please click here to view a larger version of this figure.

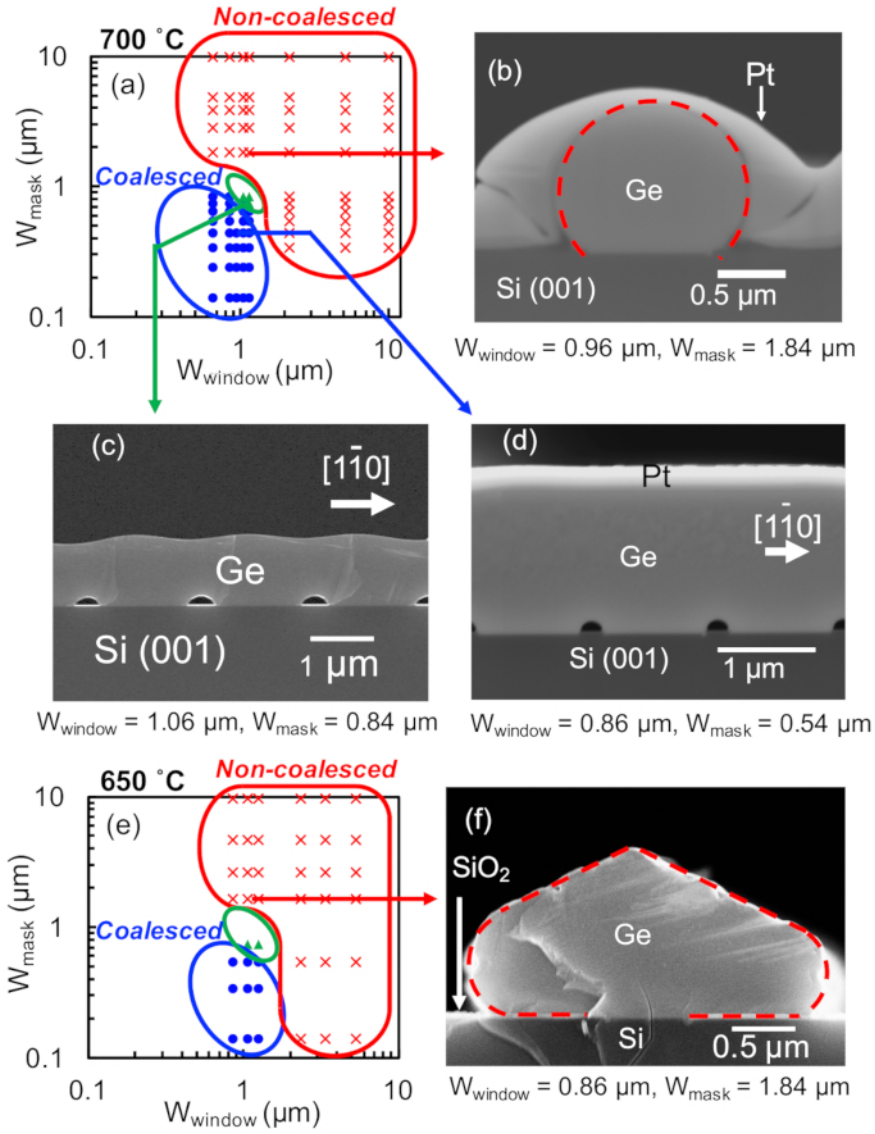

Figure 5: Distribution maps and SEM images of coalesced/non-coalesced Ge layers. Please click here to view a larger version of this figure.

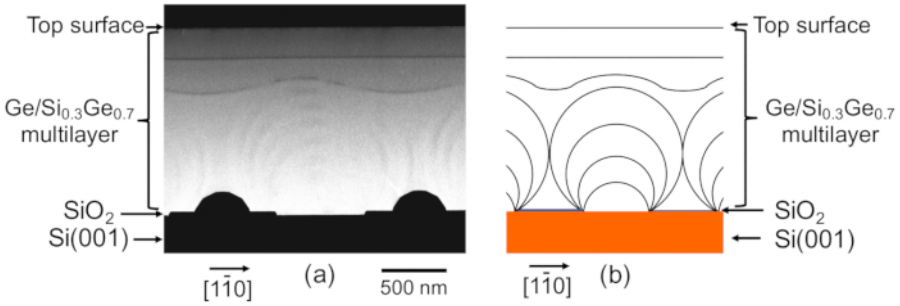

Figure 6: (a) A cross-sectional HAADF STEM image of coalesced Ge (W_{window} = 0.66 μm, W_{mask} = 0.84 μm) grown at 700 °C with 10-nm-thick $Si_{0.3}Ge_{0.7}$ demarcation layers, and (b) a schematic illustration corresponding to the conditions shown in (a). Please click here to view a larger version of this figure.

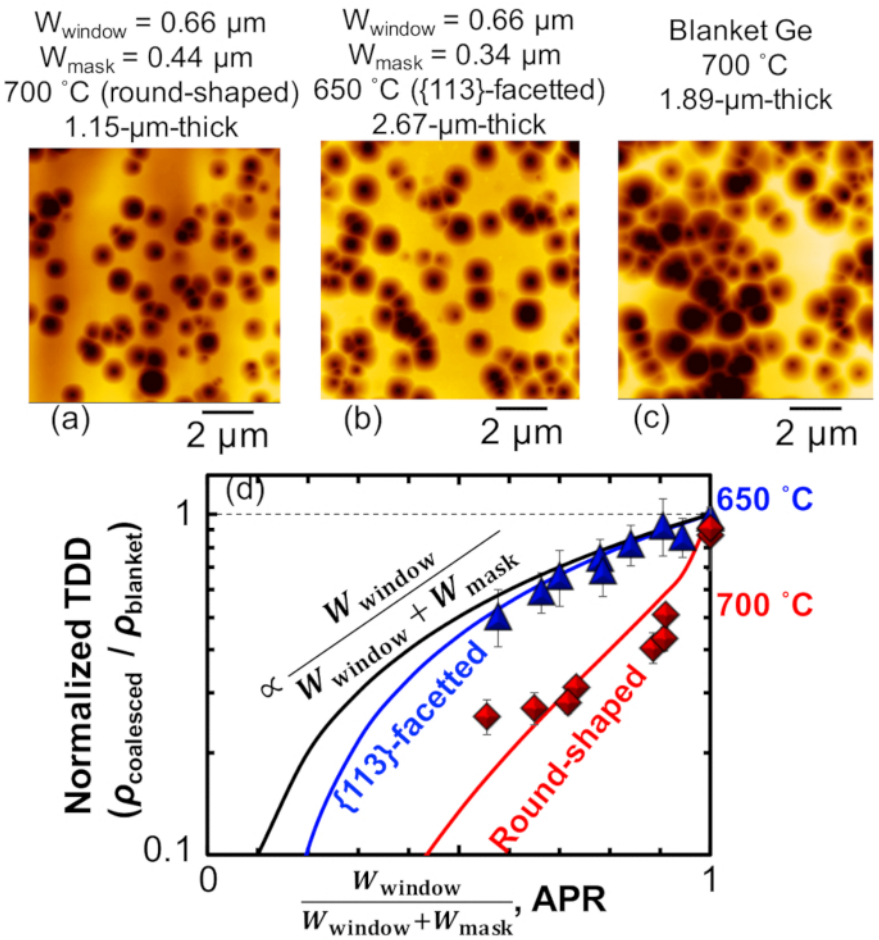

Figure 7: Typical AFM images in order to measure EPDs for (a) 1.15-μm-thick coalesced Ge grown at 700 °C (W_{window} = 0.66 μm and W_{mask} = 0.44 μm), (b) 2.67-μm-thick coalesced Ge grown at 650 °C (W_{window} = 0.86 μm and W_{mask} = 0.34 μm), and (c) 1.89-μm-thick blanket Ge grown at 700 °C, and summary of the EPD measurement results in (d). Please click here to view a larger version of this figure.

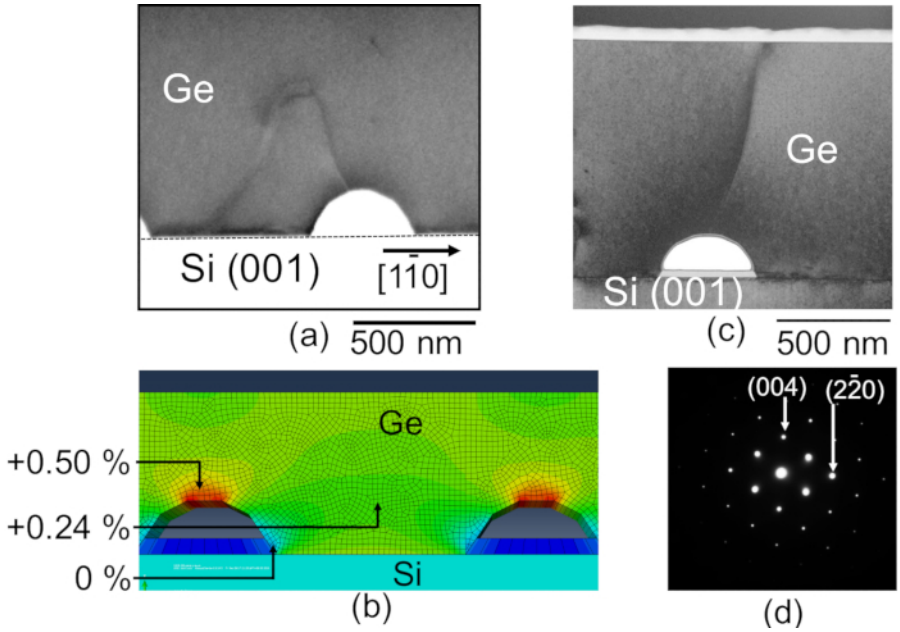

Figure 8: (110) cross-sectional (a) STEM and (b) TEM images of coalesced Ge layers (W_{window} = 0.66 μm and W_{mask} = 0.44 μm), (c) electron diffraction pattern obtained near the defect shown in (b), and (d) finite element method simulation result of a strain distribution in the coalesced Ge. Figures 9(a), (c), and (d) have been modified from [20]. Please click here to view a larger version of this figure.

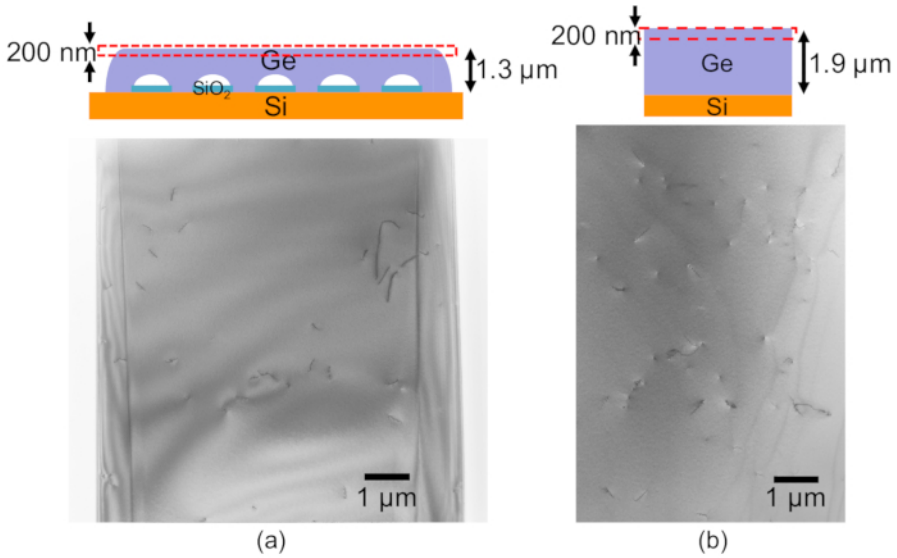

Figure 9: Bright-field plan-view TEM images of (a) a coalesced Ge layer (W_{window} = 0.82 µm, W_{mask} = 0.68 µm) and (b) a blanket Ge layer. Please click here to view a larger version of this figure.

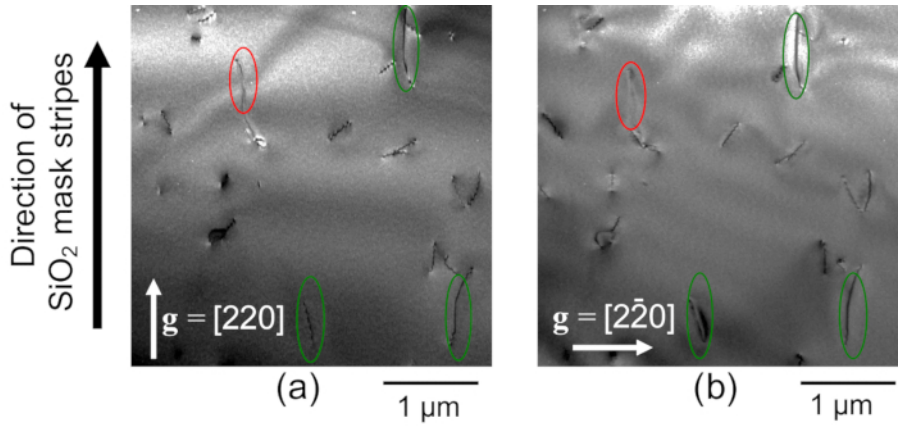

Figure 10: Plan-view TEM images of a high-TDD small area with g vectors of (a) [220] and (b) [2$\bar{2}$0]. This figure has been modified from [20]. Please click here to view a larger version of this figure.

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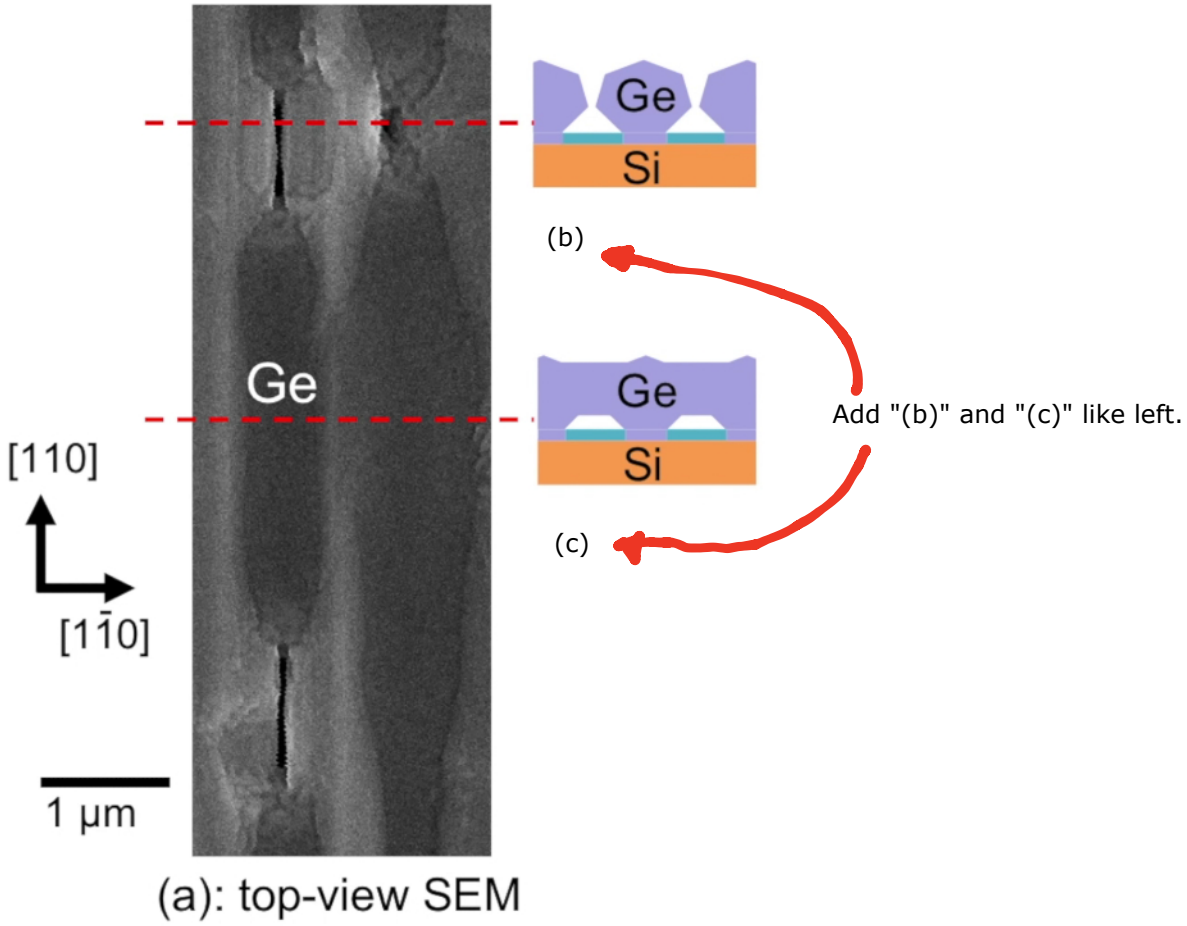

Figure 11: (a) A plan-view SEM image, (b) a bird's eye schematic image, and (c) a ($1\bar{1}0$) cross-sectional schematic image of a partially coalesced SEG Ge. This figure has been modified from [20]. Please click here to download this video.

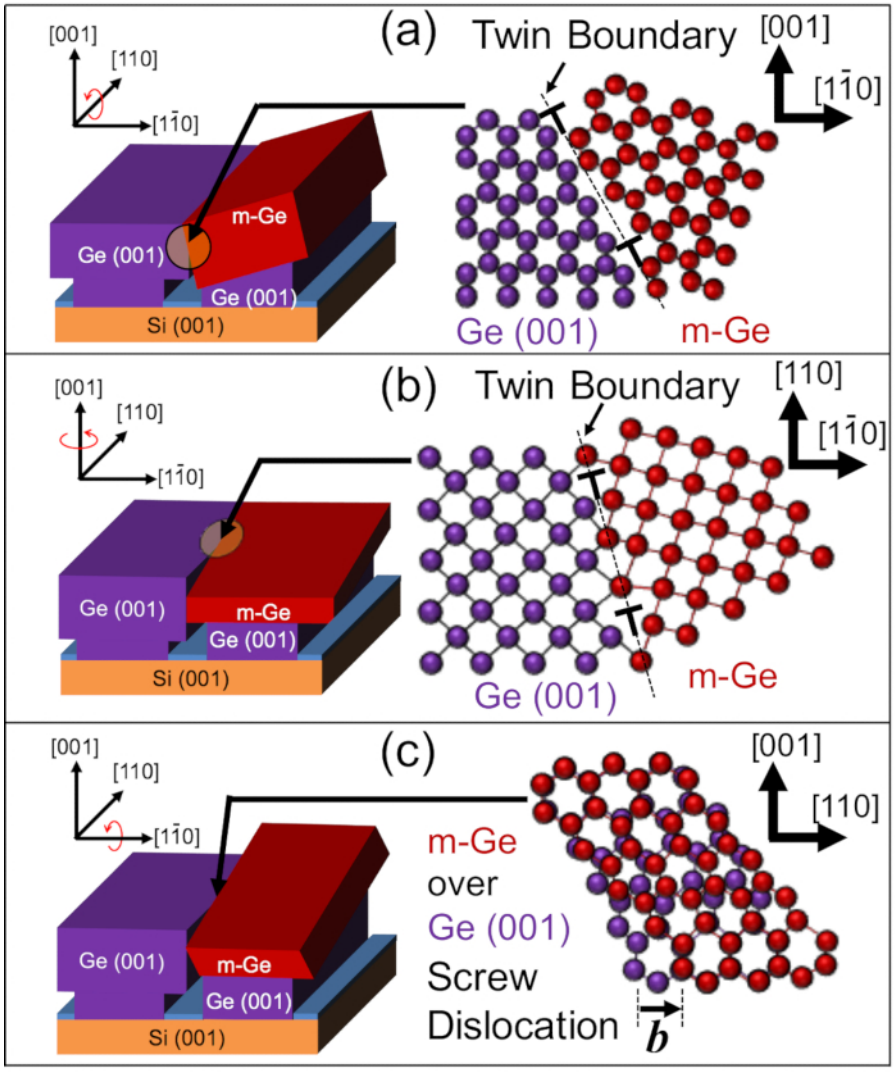

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Figure 12: Schematics of defect generation when SEG Ge layers coalesce with crystal rotation around (a) [110], (b) [001], and (c) [1$\bar{1}$0] orientation. This figure has been modified from [20]. Please click here to view a larger version of this figure.

Method	Achieved TDD (cm-2)	Temperature (˚C)	Buffer layer thickness
Thermal annealing	2e7	≈900 ˚C	≈100 nm (low-temperature buffer)
SiGe graded buffer	1e6	growth temperature (600–700 ˚C)	2–3 μm
ART	1e6	growth temperature (600–700 ˚C)	500–1000 nm
Si pillar seeds	1e5	≈800 ˚C	≈5 μm
This work	4e7	growth temperature (700 ˚C)	≈150 nm

Table 1: A summary of achieved TDD and drawbacks in view of photonic device application for conventional/presented TDD reduction methods.

Supplemental Figure 1: Four typical methods widely employed to reduce TDD in epitaxial Ge on Si: (a) thermal annealing, (b) SiGe graded buffer, (c) Aspect ratio trapping (ART), and (d) Si pillar seeds. Please click here to download this figure.

Supplemental Video 1: Schematic illustrations of a TD bent owing to image force in a round-shaped SEG Ge. Please click here to download this video.

Discussion

In the present work, TDD of 4 x 10^7/cm^2 were experimentally shown. For further TDD reduction, there are mainly 2 critical steps within the protocol: SEG mask preparation and epitaxial Ge growth.

Our model shown in **Figure 4** indicates that TDD can be reduced lower than 10^7/cm^2 in coalesced Ge when APR, $W_{window}/(W_{window} + W_{mask})$, is as small as 0.1. Toward further TDD reduction, SEG masks with smaller APR should be prepared. As mentioned in step 2.1.2, the minimum values of W_{window} and W_{mask} were 0.5 µm and 0.3 µm, respectively, limited by the resolution in the employed EB lithography system. One simple method to reduce APR is to modify lithography and etching processes (e.g., to use another photoresist, to use better lithography system, to use thinner SiO_2 layers with shallower BHF etching, etc.). Mature lithography and etching process will enable SEG masks narrower than 100 nm. In the present work, coalesced Ge with a flat top surface were obtained when $W_{mask} \leq 1$ µm. Thus, W_{window} of 100 nm and W_{mask} of 900 nm (APR = 0.1) will give us coalesced Ge with flat top surface in the present growth conditions.

In addition to that, the modification of SEG mask preparation should bring less edge undulation of SEG masks, resulting in suppression of misorientation between Ge SEG layers. The TD generation when SEG Ge layers coalesce (**Figure 11**) will be suppressed as the result of the modification of SEG mask preparation.

As revealed by calculation results (**Figure 3**), suppression of Ge growth on SiO_2 is required to reduce TDD. The suppression of Ge growth on SiO_2 is brought by modification of Ge growth step (i.e., elevation of growth temperature, rotation of SEG mask, introduction of H_2 gas, and reduction of the pressure of GeH_4 gas[44,45]).

The TDD reduction method proposed/verified in the present work is superior to existing methods in terms of application for Ge photonic devices (i.e., TDD is reduced without any thermal annealing nor thick buffer layers). The maximum process temperature was 700 °C, which is the growth temperature, and the height of the void was ≈150 nm. Compared with existing methods, the maximum temperature is lower than annealing temperature (typically 900 °C)[7], and height of the void is shallower than SiGe graded buffer layers (typically several µm)[10], SiO_2 trenches for ART (typically 0.5-1 µm)[13], and buffer layer for Ge growth on Si pillars (typically ≈5 µm)[18]. The comparison of conventional/presented methods are summarized in **Table 1**.

Considering the footprint of a typical Ge photonic device (≈100 µm^2), TDD lower than 10^6/cm^2, and a number of TD < 1/device will be the final goal. Since the theoretical limit of TDD for this method is 0, TDD lower than 10^6/cm^2 is potentially achievable. Toward the goal, more optimized lithography and etching will be investigated.

Disclosures

The authors have nothing to disclose.

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