Theoretical Calculation and Experimental Verification for Dislocation Reduction in Germanium Epitaxial Layers with Semicylindrical Voids on Silicon
--Manuscript Draft--

Article Type:	Invited Methods Article - JoVE Produced Video
Manuscript Number:	JoVE58897R3
Full Title:	Theoretical Calculation and Experimental Verification for Dislocation Reduction in Germanium Epitaxial Layers with Semicylindrical Voids on Silicon
Keywords:	Germanium; silicon; Photonics; Integrated Photonics; Devices; materials; Systems
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Additional Information:	
Question	Response
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Letter to the Editor

Title: Theoretical Calculation and Experimental Verification for Dislocation Reduction in Ge Epitaxial Layers with Semicylindrical Voids on Si
Submission number: JoVE58897

Dear Dr. Vineeta Bajaj,
Review Editor of JoVE,

We are grateful to submit our manuscript to JoVE, originally entitled "A method of dislocation reduction in Ge epitaxial layers with semicylindrical voids on Si: theoretical calculation and experimental verification," and revised to "Theoretical Calculation and Experimental Verification for Dislocation Reduction in Ge Epitaxial Layers with Semicylindrical Voids on Si."
We have revised our manuscript in response to the editorial comments, and prepared a manuscript for review. Important changes and added descriptions are highlighted by RED color in the revised manuscript for review.

[Comments]
Changes to be made by the author(s) regarding the manuscript:
1. Please take this opportunity to thoroughly proofread the manuscript to ensure that there are no spelling or grammar issues.
2. Please revise lines 308-310 to avoid previously published text.

[Reply]
We have revised the lines 308–310 (lines 366–368 in the revised manuscript) to avoid previously published text. Thank you for the comment.

[Comment]
3. Please obtain explicit copyright permission to reuse any figures from a previous publication. Explicit permission can be expressed in the form of a letter from the editor or a link to the editorial policy that allows re-prints. Please upload this information as a .doc or .docx file to your Editorial Manager account. The Figure must be cited appropriately in the Figure Legend, i.e. "This figure has been modified from [citation]."

[Reply]
We have revised the figure captions, and uploaded the information of copyright permission for the reuse of figures from a previous publication [20] in the revised manuscript.
[20] Yako, M., Ishikawa, Y., Abe, E., Wada, K., Defects and Their Reduction in Ge Selective Epitaxy and Coalescence Layer on Si With Semicylindrical Voids on SiO_2 Masks, *IEEE Journal of Selected Topics in Quantum Electronics*, 24 (6), 8201007 (2018).

[Comments]
4. Please ensure that the figures are properly labeled and match their corresponding

figure legends. See some inconsistencies listed below.

5. Figure 3: The uploaded Figure 3 does not match the description in figure legend. Please revise.

6. Figure 4: The uploaded Figure 4 seems to match figure legend of Figure 3.

7. Figures 6 and 8: Please use "°C" for the temperature unit and include a space between numbers and their units (700 °C, etc.).

8. Figure 11: Please describe what the green and red ellipses stand for.

9. What is the difference between Figure 2 and Figure 2R? Please upload only one Figure 2.

10. Please reference Figure 2 and Figure 7 in the manuscript. Please number the figures in the sequence in which you refer to them in the manuscript text.

[Reply]

For Figs. 3 and 4 (Figs. 4 and 5 in the revised manuscript): we have checked the figure labels and now they are correctly labeled.

Figures 6 and 8 (Figs. 7 and 9 in the revised manuscript) are revised to use "°C" and include a space between numbers and their units.

We have added descriptions for green and red ellipses in Fig. 11 (Fig. 12 in the revised manuscript) in the revised manuscript (lines 489–493, highlighted by RED color).

We are afraid there were some mistakes in uploading the figures/movies in the last submission. We believe they are submitted correctly and there is no "Figure 2R" this time.

In the revised manuscript, Fig. 2 is referred in "PROTOCOL" part (lines 110, 114, and 118), and Fig. 7 (Fig. 8 in the revised manuscript) is referred in "REPRESENTATIVE RESULTS" part (from line 341). Please find the RED colored text showing where they are referred.

[Comment]

11. Table of Materials: Please revise to include the name, company, and catalog number of all relevant supplies, reagents, equipment and software in separate columns in an xls/xlsx file. Please sort the items in alphabetical order according to the name of material/equipment.

[Reply]

We have revised the Table of Materials to include the detailed information of the material/equipment used in the experiments.

[Comments]

12. Please revise the title to avoid the use of colon.

[Reply]

We have revised the title as

"Theoretical Calculation and Experimental Verification for Dislocation Reduction in Ge Epitaxial Layers with Semicylindrical Voids on Si"

to avoid the use of colon.

[Comment]
13. Please revise the protocol text to avoid the use of any personal pronouns (e.g., "we", "you", "our" etc.).

[Reply]
We have revised the PROTOCOL part and removed all personal pronouns from the revised manuscript.

[Comments]
14. Please add more details to your protocol steps. There should be enough detail in each step to supplement the actions seen in the video so that viewers can easily replicate the protocol. Please ensure you answer the "how" question, i.e., how is the step performed? Alternatively, add references to published material specifying how to perform the protocol action. See examples below.
15. 2.1.1: Please specify the mass/size of the substrates used.
16. 2.1.2: Please describe how electron beam (EB) lithography and wet etching are done.
17. 2.1.3: How to set different parameters?
18. 2.1.4: Please describe how to prepare square-shaped Si window areas of 4 mm in width. What parameters are set differently?
19. 2.1.5: Do the Si wafers refer to product from 2.1.3 or 2.1.4 or both? Please specify the concentration of HF used.
20. 2.2.1-2.2.5: Please reorganize these steps so that they can be followed in chronological order.
21. 2.2.5: Please describe how to perform periodic insertion of 10-nm-thick Si0.3Ge0.7 demarcation layers.
22. 2.3.2: Please describe how this is done.

[Reply]
We have added more details in protocol steps.
Answer for each question:
15: 4 inch Si substrates were used (section 2.1.4 in the revised manuscript).
16: more details in EB lithography (sections 2.1.6–2.1.10) and wet etching (sections 2.1.11–2.1.13) have been described in the revised manuscript.
17 and 18: the SEG mask design was determined by creating design file. We have added description about creating the design file (sections 2.1.1–2.1.3) in the revised manuscript.
19: The Si wafers are the same one described in the former sections. In fact, we used both the words "wafer" and "substrate" for the same thing. In the revised manuscript, we use only "substrate". The concentration of HF for the each step is added in the revised manuscript.
20: We have added more detail of Ge growth protocol in section 2.2.1–2.2.6.
21: 10-nm-thick $Si_{0.3}Ge_{0.7}$ layers were inserted by just introducing Si_2H_6 gas in Ge growth chamber. We have added a description in section 2.2.6.
22. We have added more detailed description about EPD measurements in section 2.3.1–2.3.4.

[Comment]

23. JoVE articles are focused on the methods and the protocol, thus the discussion should be similarly focused. Please revise the Discussion to explicitly cover the following in detail in 3-6 paragraphs with citations:

a) Critical steps within the protocol

b) Any modifications and troubleshooting of the technique

c) Any limitations of the technique

d) The significance with respect to existing methods

e) Any future applications of the technique

[Reply]

We have revised the discussion part so as to focus on the points a)–e) above.

a) Critical steps within the protocol are (A) SEG mask preparation and (B) epitaxial Ge growth, as mentioned in lines 560–562 (highlighted by RED color).

Then, b) and c) are described for each steps (lines 564–583).

d) is described in lines 585–593 and Table 1, and e) is described in lines 598–601.

[Comment]

24. Please ensure that the references appear as the following: [Lastname, F.I., LastName, F.I., LastName, F.I., LastName, F.I. Article Title. Source. Volume (Issue), FirstPage – LastPage (YEAR).] For more than 6 authors, list only the first author then et al. Please do not abbreviate journal titles. See the example below:

Bedford, C.D., Harris, R.N., Howd, R.A., Goff, D.A., Koolpe, G.A. Quaternary salts of 2-[(hydroxyimino)methyl]imidazole. Journal of Medicinal Chemistry. 32 (2), 493-503 (1998).

[Reply]

We have revised the form of references as pointed out.

Thank you again for your kind support and consideration on our submission to JoVE.

For the payment: since fiscal year in Japan starts from April, our budget requests us to pay before the end of February.
We would be grateful if you would kindly take into account the situation for the final judgement.

<div style="text-align:right">

Sincerely,

Motoki Yako

Ph.D. candidate
Department of Materials Engineering
University of Tokyo

</div>

1　**TITLE:**
2　Theoretical Calculation and Experimental Verification for Dislocation Reduction in Germanium
3　Epitaxial Layers with Semicylindrical Voids on Silicon
4
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27　**SUMMARY:**
28　Theoretical calculation and experimental verification are proposed for a reduction of threading
29　dislocation (TD) density in germanium epitaxial layers with semicylindrical voids on silicon.
30　Calculations based on the interaction of TDs and surface via image force, TD measurements, and
31　transmission electron microscope observations of TDs are presented.
32

33　**ABSTRACT:**
34　Reduction of threading dislocation density (TDD) in epitaxial germanium (Ge) on silicon (Si) has
35　been one of the most important challenges for the realization of monolithically integrated
36　photonics circuits. The present paper describes methods of theoretical calculation and
37　experimental verification of a novel model for the reduction of TDD. The method of theoretical
38　calculation describes the bending of threading dislocations (TDs) based on the interaction of TDs
39　and non-planar growth surfaces of selective epitaxial growth (SEG) in terms of dislocation image
40　force. The calculation reveals that the presence of voids on SiO_2 masks help to reduce TDD.
41　Experimental verification is described by germanium (Ge) SEG, using an ultra-high vacuum
42　chemical vapor deposition method and TD observations of the grown Ge via etching and cross-
43　sectional transmission electron microscope (TEM). It is strongly suggested that the TDD reduction
44　would be due to the presence of semicylindrical voids over the SiO_2 SEG masks and growth

45 temperature. For experimental verification, epitaxial Ge layers with semicylindrical voids are
46 formed as the result of SEG of Ge layers and their coalescence. The experimentally obtained TDDs
47 reproduce the calculated TDDs based on the theoretical model. Cross-sectional TEM observations
48 reveal that both the termination and generation of TDs occur at semicylindrical voids. Plan-view
49 TEM observations reveal a unique behavior of TDs in Ge with semicylindrical voids (i.e., TDs are
50 bent to be parallel to the SEG masks and the Si substrate).
51
52 **INTRODUCTION:**
53 Epitaxial Ge on Si has attracted substantial interests as an active photonic device platform since
54 Ge can detect/emit light in the optical communication range (1.3–1.6 µm) and is compatible with
55 Si CMOS (complementary metal oxide semiconductor) processing techniques. However, since the
56 lattice mismatch between Ge and Si is as large as 4.2%, threading dislocations (TDs) are formed
57 in Ge epitaxial layers on Si at a density of ~10^9/cm^2. The performances of Ge photonic devices are
58 deteriorated by TDs because TDs works as carrier generation centers in Ge photodetectors (PDs)
59 and modulators (MODs), and as carrier recombination centers in laser diodes (LDs). In turn, they
60 would increase reverse leakage current (J_{leak}) in PDs and MODs[1–3], and threshold current (J_{th}) in
61 LDs[4–6].
62
63 Various attempts have been reported to reduce TD density (TDD) in Ge on Si (**Supplemental**
64 **Figure 1**). Thermal annealing stimulates movement of TDs leading to the reduction of TDD,
65 typically to 2 x 10^7/cm^2. The drawback is the possible intermixing of Si and Ge and out-diffusion
66 of dopants in Ge such as phosphorus[7–9] (**Supplemental Figure 1a**). The SiGe graded buffer layer[10–
67 12] increases the critical thicknesses and suppresses the generation of TDs leading to the reduction
68 of TDD, typically to 2 x 10^6/cm^2. The drawback here is that the thick buffer reduces light coupling
69 efficiency between Ge devices and Si waveguides underneath (**Supplemental Figure 1b**). Aspect
70 ratio trapping (ART)[13–15] is a selective epitaxial growth (SEG) method and reduces TDs by trapping
71 TDs at the sidewalls of thick SiO$_2$ trenches, typically to <1 x 10^6/cm^2. The ART method uses a thick
72 SiO$_2$ mask to reduce TDD in Ge over the SiO$_2$ masks, which locates far above Si and have the same
73 drawback (**Supplemental Figure 1b,1c**). Ge growth on Si pillar seeds and annealing[16–18] are similar
74 to the ART method, enabling TD trapping by the high aspect ratio Ge growth, to <1 x 10^5/cm^2.
75 However, high temperature annealing for Ge coalescence has the same drawbacks in
76 **Supplemental Figure 1a–c** (**Supplemental Figure 1d**).
77
78 To achieve low-TDD Ge epitaxial growth on Si that is free from the drawbacks of the above-
79 mentioned methods, we have proposed coalescence-induced TDD reduction[19,20] based on the
80 following two key observations reported so far in SEG Ge growth[7,15,21–23]: 1) TDs are bent to be
81 normal to the growth surfaces (observed by the cross-sectional transmission electron microscope
82 (TEM)), and 2) coalescence of SEG Ge layers results in the formation of semicylindrical voids over
83 the SiO$_2$ masks.
84
85 We have assumed that the TDs are bent owing to the image force from the growth surface. In
86 the case of Ge on Si, the image force generates 1.38 GPa and 1.86 GPa shear stresses for screw
87 dislocations and edge dislocations at distances 1 nm away from the free surfaces, respectively[19].
88 The calculated shear stresses are significantly larger than the Peierls stress of 0.5 GPa reported

89   for 60° dislocations in Ge[24]. The calculation predicts TDD reduction in Ge SEG layers on a
90   quantitative basis and is in good agreement with the SEG Ge growth[19]. TEM observations of TDs
91   are carried out to understand TD behaviors in the presented SEG Ge growth on Si[20]. The image-
92   force-induced TDD reduction is free from any thermal annealing or thick buffer layers, and thus
93   is more suitable for photonic device application.

94

95   In this article, we describe specific methods for the theoretical calculation and experimental
96   verification employed in the proposing TDD reduction method.

97

98   **PROTOCOL:**

99

100   **1. Theoretical calculation procedure**

101

102   1.1. Calculate trajectories of TDs. In the calculation, assume the SEG masks to be thin enough to
103   ignore the ART effect on TDD reduction.

104

105   1.1.1. Determine growth surfaces and express them by equation(s). For instance, express the
106   time evolution of a round-shaped cross-section of a SEG Ge layer with the time evolution
107   parameter $n = i$, SEG Ge heights (h_i) and SEG Ge radii (r_i), as shown in the **Supplemental Video**
108   **1a** and Eq. (1):

109

110   $$x^2 + \{y - (r_i - h_i)\}^2 = r_i^2 . \quad (1)$$

111

112   1.1.2. Determine normal directions for an arbitrary location on the growth surfaces. For the
113   round-shaped cross-section SEG Ge, describe the normal line at (x_i, y_i) as $y = \frac{y_i - (h_i - r_i)}{x_i} x +$
114   $h_i - r_i$, shown in **Supplemental Video 1b** as a red line. Then, obtain the edge of the TD (x_{i+1},
115   y_{i+1}) from the point (x_i, y_i) by solving the following simultaneous equations:

116

117   $$\begin{cases} x^2 + \{y - (r_{i+1} - h_{i+1})\}^2 = r_{i+1}^2 & (2a) \\ y = \dfrac{y_i - (h_i - r_i)}{x_i} x + h_i - r_i & (2b) \end{cases}$$

118

119   1.1.3. Calculate a trajectory of one TD depending on the location of TD generation (x_0, 0), as
120   shown in **Supplemental Video 1c**. In other words, a trajectory for an arbitrary TD can be
121   calculated by the method described above.

122

123   1.1.4. Calculate TDD assuming that TDs penetrate to the bottom surface and contribute to the
124   reduction of TDD (i.e., TDs below the point where SEG Ge layers coalesce are trapped by
125   semicylindrical voids and never appear on the top surface).

126

127   **2. Experimental verification procedure**

128

129   2.1. SEG mask preparation

130

131   2.1.1. Prior to the fabrication of SEG masks, define Ge growth areas by preparing a design file. In
132   the present work, prepare line-and-space patterns aligned to the [110] direction and square-
133   shaped Si window areas of 4 mm in width using commercial software (e.g., AutoCAD).

134

135   2.1.2. Determine the design of SEG masks (in particular W_{window} and W_{mask}) using the software.
136   W_{window} is the window width (Si seed width) and W_{mask} is the SiO_2 mask width, such that SEG Ge
137   layers can coalesce with their adjacent ones. Determine W_{window} and W_{mask} by drawing rectangles
138   by clicking **open file → structure → rectangle or polyline**.

139

140   NOTE: The width of the rectangles becomes W_{window}, and the interval of the rectangles becomes
141   W_{mask}. In the present work, the minimum values of W_{window} and W_{mask} are 0.5 μm and 0.3 μm,
142   respectively, which are restricted by the resolution in the employed EB lithography system.

143

144   2.1.3. As references, draw square-shaped Si window areas of 4 mm in width D, regarded as the
145   blanket areas. Click **open file → structure → rectangle or polyline** to draw the square-shaped Si
146   window. Use the schematics shown in **Figure 1** to prepare the line-and-space patterns and the 4
147   mm square blanket area.

148

149   2.1.4. Prepare B-doped p-Si (001) substrates with the resistivity of 1–100 Ω·cm. In the present
150   work, use 4-inch Si substrates. Clean the substrate surfaces with Piranha solution (a mixture of
151   20 mL of 30% H_2O_2 and 80 mL of 96% H_2SO_4) as necessary.

152

153   2.1.5. Open the lid on a tube furnace and load the Si substrates into the furnace using a glass rod.
154   In the present work, oxidize 10 Si substrates at one time.

155

156   2.1.6. Start to blow dry N_2 gas into the furnace by opening the gas valve. Then, set the gas flow
157   rate to 0.5 L/m by controlling the valve.

158

159   2.1.7. Set the annealing temperature by changing the program. In the present work, use "pattern
160   step (mode 2)" and set the process temperature to 900 °C. Then, run the program by pushing
161   **function → run**.

162

163   2.1.8. As the temperature reaches 900 °C, close the dry N_2 valve, open the dry O_2 valve (O_2 flow
164   = 1 L/m), and keep for 2 h.

165

166   NOTE: Perform steps 2.1.9–2.1.16 in a yellow room.

167

168   2.1.9. Coat the oxidized Si substrates with a surfactant (OAP) using a spin coater and then bake
169   at 110 °C for 90 s on a hotplate.

170

171   2.1.10. After the surfactant coating, coat the Si substrates with a photoresist (e.g., ZEP520A) using
172   a spin coater and then bake at 180 °C for 5 min on a hotplate.

173

174 2.1.11. Load the Si substrates with the surfactant and photoresist into an electron beam (EB)
175 writer.

177 2.1.12. Read the design file (prepared in step 2.1.2) in the EB writer and make an operation file
178 (WEC file). Set dose quantity as 120 $\mu C/cm^2$ in the WEC file. As the substrate loading finishes,
179 perform EB exposure by clicking the **single exposure** button.

181 2.1.13. Unload the substrate from the EB writer by clicking **wafer carry → unload** as the exposure
182 finishes.

184 2.1.14 Prepare a photoresist developer (ZED) and a rinse for the developer (ZMD) in a draft
185 chamber. Dip the exposed Si substrates into the developer for 60 s at room temperature.

187 2.1.15. Remove the Si substrates from the developer, and then dry the substrate with N_2 gas.

189 2.1.16. Put the developed Si substrates on a hotplate to bake at 110 °C for 90 s.

191 2.1.17. Dip the Si substrates into a buffered hydrofluoric acid (BHF-63SE) for 1 min in order to
192 remove part of the SiO_2 layers exposed to the air as the result of EB exposure and development.

194 2.1.18. Remove the photoresist from the Si substrates by dipping into an organic photoresist
195 remover (e.g., Hakuri-104) for 15 min.

197 2.1.19. Dip the Si substrates into 0.5% diluted hydrofluoric acid for 4 min to remove the thin
198 native oxide in the window regions but to retain the SiO_2 masks. Then load onto an ultrahigh-
199 vacuum chemical vapor deposition (UHV-CVD) chamber to grow Ge. **Figure 2** shows the UHV-
200 CVD system used in the present work.

202 2.2. Epitaxial Ge growth

204 2.2.1. Load the Si substrate with SEG masks (fabricated as in step 2.1) into a load lock chamber.

206 2.2.2. Set the buffer/main growth temperature in the **Recipe** tab shown on the operation
207 computer. Determine the durations for the main growth of Ge so that SEG Ge layers coalesce
208 with adjacent ones. To decide the durations for the main growth, consider the growth rate of Ge
209 on the {113} planes, which determines the growth in the in-plane/lateral direction[26]. In the
210 present work, set the durations for the main growth as 270 min and 150 min for 650 °C and 700
211 °C, respectively.

213 2.2.3. Click **start** in main window, and then the Si substrate is automatically transferred into the
214 growth chamber.

216 NOTE: Protocol on epitaxial Ge growth (steps 2.2.4–2.2.7) is automatically processed.

218 2.2.4. Grow Ge buffer on the loaded Si substrate at low-temperature (≈380 °C). Use GeH_4 diluted
219 at 9% in Ar as the source gas and keep the partial pressure of GeH_4 for 0.5 Pa during the buffer
220 growth.

221

222 2.2.5. Grow Ge main layer at an elevated temperature. Keep the partial pressure of GeH_4 for 0.8
223 Pa during the main growth. In the present work, use two different temperatures of 650 and 700
224 °C for the main growth temperature in order to compare SEG Ge with a round-shaped cross-
225 section and with a {113}-facetted cross-section[25].

226

227 NOTE: The growth rate of Ge on the (001) plane was 11.7 nm/min independent of the
228 temperature.

229

230 2.2.6. In order to visualize the evolution of SEG Ge and their coalescence, perform Ge growth
231 with periodic insertion of 10-nm-thick $Si_{0.3}Ge_{0.7}$ demarcation layers on another Si substrate.
232 $Si_{0.3}Ge_{0.7}$ layers were formed using Si_2H_6 and GeH_4 gases. During the $Si_{0.3}Ge_{0.7}$-layer growth, set
233 the partial pressure of Si_2H_6 gas at 0.02 Pa and the partial pressure of GeH_4 gas at 0.8 Pa.

234

235 2.2.7. As the Si substrate is automatically transferred from the growth chamber to the load lock
236 chamber, vent the load lock chamber and unload the Si substrate manually.

237

238 2.3. Etch pit density (EPD) measurements

239

240 2.3.1. Dissolve 32 mg of I_2 in 67 mL of CH_3COOH using an ultrasonic cleaning machine.

241

242 2.3.2. Mix the I_2-dissolved CH_3COOH, 20 mL of HNO_3, and 10 mL of HF.

243

244 2.3.3. Dip the Ge-grown Si substrates into the $CH_3COOH/HNO_3/HF/I_2$ solution for 5–7 s in order
245 to form etched pits.

246

247 2.3.4. Observe the etched Ge surfaces with an optical microscope (typically 100x) to ensure that
248 etched pits are successfully formed.

249

250 2.3.5. Employ an atomic force microscope (AFM) to count the etched pits. Put the etched Ge
251 sample on an AFM stage, and then approach the probe by clicking **auto approach**.

252

253 2.3.6. Decide the observation area using an optical microscope integrated with an AFM, and scan
254 five different 10 µm x 10 µm areas. The amplitude damping factor is automatically determined.

255

256 2.4. TEM observations

257

258 2.4.1. Pick up TEM specimens from the coalesced/blanket Ge layers by using a focused Ge ion
259 beam (FIB micro sampling method)[27].

260

261 2.4.2. Polish the TEM specimens in an ion milling system using Ar ions. In the present work, thin

262   down TEM specimens for cross-sectional observations to be 150–500 nm in the [110] direction,
263   and for plan-view observations to be 200 nm in the [001] direction.

264

265   2.4.3. For plan-view TEM specimens, protect the top surfaces of the Ge layers with amorphous
266   layers, and then thin down from the bottom (substrate) side of the Ge layers.

267

268   2.4.4. Perform TEM observations under an acceleration voltage of 200 kV. Perform cross-
269   sectional bright-field scanning TEM (STEM) observations in order to observe thick (500 nm) TEM
270   specimens.

271

272   2.4.5. For a coalesced Ge with $Si_{0.3}Ge_{0.7}$ demarcation layers, perform cross-sectional high-angle
273   annular dark field (HAADF) STEM observations under an acceleration voltage of 200 kV.

274

275   **REPRESENTATIVE RESULTS:**
276   **Theoretical Calculation**
277   **Figure 3** shows calculated trajectories of TDs in 6 types of coalesced Ge layers: here, we define
278   the aperture ratio (APR) to be $W_{window}/(W_{window} + W_{mask})$. **Figure 3a** shows a round-shaped SEG
279   origin coalesced Ge of APR = 0.8. Here, 2/6 TDs are trapped. **Figure 3b** shows a {113}-facetted
280   SEG origin coalesced Ge of APR =0.8. Here, 0/6 TDs are trapped. **Figure 3c** shows a round-shaped
281   SEG origin coalesced Ge of APR = 0.1. Here, 5/6 TDs are trapped. **Figure 3d** shows a {113}-facetted
282   SEG origin coalesced Ge of APR = 0.1. Here, 6/6 TDs are trapped. **Figure 3e** shows a round-shaped
283   SEG origin coalesced Ge of APR = 0.1, in case that Ge grows on SiO_2 masks. Here, 0/6 TDs are
284   trapped. **Figure 3f** shows a {113}-facetted SEG origin coalesced Ge of APR = 0.1, in case that Ge
285   grows on SiO_2 masks. Here, 0/6 TDs are trapped.

286

287   The trajectories of 6 TDs generated at $(x_0, 0)$, where x_0 = 0.04, 0.1, 0.2, 0.4, 0.6, and 0.8 times
288    $W_{window}/2$, are shown as red lines in each figure. TDs located above the coalescence points of
289   these two SEG Ge layers propagate upward to the top surface, while TDs below the points
290   propagate downward to remain at the void surface over the SiO_2 mask.

291

292   In **Figure 3a–3d**, it is assumed that SEG Ge does not grow on SiO_2. Thus, the sidewalls of the {113}-
293   facetted SEG Ge are assumed to be round-shaped in order to not touch the SiO_2 masked area. It
294   is clearly shown that round-shaped SEG and then coalesced Ge are more effective to reduce TDD
295   at an APR of 0.8, than the {113}-facetted case, while {113}-facetted and then coalesced Ge are
296   more effective than a round-shaped one at an APR of 0.1. This "crossing" is ascribed to the
297   presence of {113} facets near the SEG top: {113} facets are more deviated from the [001]
298   direction than round-shaped surfaces.

299

300   **Figure 3e and Figure 3f** show coalesced Ge at an aperture ratio of 0.1, assuming that Ge is not
301   nucleated on SiO_2 but shows wetting with the SiO_2 mask, widely reported in previously reported
302   Ge coalescence[13,15,22,28–31]. As shown in **Figure 3e and Figure 3f**, there is no semi cylindrical void
303   between two SEG and thus no TD is trapped at the surface.

304

305   **Figure 4** shows calculated TDDs in coalesced Ge. In **Figure 4**, the red line shows calculated TDDs

306   in coalesced Ge originating from the round-shaped SEG Ge, and the blue line shows calculated
307   TDDs in coalesced Ge originating from the {113}-facetted SEG Ge. Since TDs in Ge on Si originate
308   from the lattice mismatch between Ge and Si, it is assumed that TD generation occurs only at
309   interfaces between Ge and Si. In other words, TDD should be reduced with APR.
310
311   When APR is larger than 0.11, the round-shaped SEG Ge is more effective than the {113}-facetted
312   one (**Figure 3a and Figure 3b**). When APR is smaller than 0.11, on the other hand, the {113}-
313   facetted SEG Ge becomes more effective than the round-shaped one (**Figure 3c and Figure 3d**).
314   As in **Figure 3**, such crossing is ascribed to the presence of {113} facets near the SEG top ($x_0 \approx 0$).
315   Note that **Figure 3e and Figure 3f** correspond to the black line in **Figure 4**, showing the reduction
316   of TDD from the reduction of APR, but not to the coalescence (i.e., SEG Ge wetting with SiO_2 has
317   a negative effect against the TDD reduction).
318
319   **Experimental Verification**
320   **Figure 5** show typical cross-sectional scanning electron microscopy (SEM) images (**Figure 5b–5d,**
321   **5f**) and the distribution maps (**Figure 5a, 5e**) showing whether coalescence occurs or not. **Figure**
322   **5b–5d**, **5f** show cross-sectional SEM images of non-coalesced SEG Ge layers (**Figure 5b**, grown at
323   700 °C; **Figure 5f**, grown at 650 °C), coalesced SEG Ge layers with a non-flat top surface (**Figure**
324   **5c**, grown at 700 °C), and coalesced SEG Ge layers with a flat top surface (**Figure 5d**; grown at 700
325   °C). SEM images shown in **Figure 5b** and **Figure 5d** are polished by a focused ion beam after
326   deposition of Pt protection layers. The coalescence occurs when the W_{window} and W_{mask} are
327   smaller than 1 µm for the present growth conditions. The SEG masks with W_{mask} of 1 µm or larger
328   prevent the coalescence of Ge due to the small amount of Ge growth in the lateral direction[26].
329   The SEG masks with a W_{window} of 2 µm or greater also prevent the coalescence of Ge, although
330   the coalescence took place when the W_{window} is smaller than 1 µm. This is because the lateral
331   growth rate of Ge over SiO_2 depends on the W_{window}[30]. The mask and window pattern dependence
332   are summarized in **Figure 7a** (700 °C) and **Figure 7e** (650 °C).
333
334   Comparing the non-coalesced SEG Ge layers (**Figure 4b and Figure 4f**), it is clearly shown that the
335   SEG Ge layer grown at 700 °C has a round-shaped cross-section while the SEG Ge layer grown at
336   650 °C has a {113}-facetted cross-section. As in **Figure 5b**, the growth at 700 °C shows a round-
337   shaped SEG Ge without Ge growth on SiO_2 (i.e., no wetting with the SiO_2 mask). Therefore, the
338   growth proceeds like **Figure 3a** and **Figure 3c**. On the other hand, as in **Figure 5f,** an {113}-
339   facetted SEG Ge appears at 650 °C. It is strongly suggestive that the Ge would show wetting with
340   the SiO_2 mask. In contrast, the edge is round-shaped (i.e., not wetting). Therefore, the growth at
341   650 °C is in between **Figure 3b** (no wetting) and **Figure 3f** (perfect wetting). This indicates that
342   the TDD reduction should be in between **Figure 3b** and **Figure 3f**. Considering the theoretical
343   results shown in **Figure 6**, these differences in the SEG Ge cross-sections should strongly influence
344   TDDs in the coalesced Ge layers.
345
346   The difference in wetting growth on SiO_2 can be understood as follows. The contact angle
347   between Ge and SiO_2 (θ) is determined by Young's equation:
348
349   $$\gamma_{SiO2} = \gamma_{Ge} \cos \theta + \gamma_{int} \quad (4)$$

350

351 Here, γ_{SiO2}, γ_{Ge}, and γ_{int} are SiO_2 surface free energy, Ge surface free energy, and Ge/SiO_2

352 interfacial free energy, respectively. The angle of the SEG Ge sidewall becomes larger as Ge

353 growth proceeds. When the angle of the SEG Ge sidewall reaches the contact angle θ, the SEG

354 Ge needs to grow in the vertical ([001]) or lateral ([$1\bar{1}0$]) direction. In the case for 650 °C growth,

355 the vertical growth is severely limited by the {113} facets, and thus SEG Ge prefers to grow in

356 lateral direction (i.e., wetting growth). Even though the wetting could generate dislocations at

357 the Ge and SiO_2 interface, it is finally to be terminated at the semicylindrical void surface. In the

358 case for 700 °C growth, Ge can grow in a vertical direction, and the contact angle is larger than

359 that for 650 °C because of a larger γ_{int}. This would be the reason why 650 °C-grown Ge shows

360 wetting over SiO_2 while 700 °C grown-Ge does not.

361

362 For Ge after coalescence, the cross-sectional structure is not influenced by the growth

363 temperature: coalesced Ge layers grown at 650 °C and the ones grown at 700 °C could not be

364 differentiated by cross-sectional SEM observations.

365

366 Note that for the fabricated patterns, W_{window} values were larger and W_{mask} values were smaller

367 than the designed ones because an isotropic wet etching process was employed to fabricate the

368 mask. The actual values of W_{window} and W_{mask} were obtained by cross-sectional SEM observations

369 after Ge growth.

370

371 In addition to that, the thickness of the mask SiO_2 layers was 30 nm according to the cross-

372 sectional SEM observations and spectroscopic ellipsometry measurements. Such thin SiO_2 layers

373 were employed to examine the TDD reduction explained in **Figure 3** and **Figure 4**, removing the

374 effect of epitaxial necking on the ART. In the present work, the aspect ratios are lower than 0.05,

375 which is small enough to ignore the effect of epitaxial necking on the ART.

376

377 **Figure 6a** shows a cross sectional HAADF STEM for a SEG with $Si_{0.3}Ge_{0.7}$ demarcation layers, and

378 a schematic illustration of **Figure 6a** is shown in **Figure 6b** (W_{window} = 0.66 μm, W_{mask} = 0.84 μm).

379 The $Si_{0.3}Ge_{0.7}$ demarcation layers clearly show the surface shapes during the growth at 700 °C.

380 The STEM image shows the Ge surfaces of each growth step from round-shaped SEG to a flat

381 epitaxial layer formed after the coalescence. The growth rate just after coalescence is strongly

382 enhanced at the coalesced areas. This rapid growth is probably induced by the Ge epilayer,

383 minimizing its surface area to get energetically stabilized.

384

385 In contrast to the pure Ge SEG, the presented Ge SEG with the $Si_{0.3}Ge_{0.7}$ demarcation layers show

386 wetting with the SiO_2 masks (**Figure 8a**). The difference in wetting is perhaps due to the insertion

387 of $Si_{0.3}Ge_{0.7}$ demarcation layers, whose nucleation is enhanced on SiO_2 layers unlikely that of Ge.

388

389 Flat-top coalesced Ge (blue-circled areas in **Figure 5a** and **Figure 5e**) are used for EPD

390 measurements. The Ge layers were etched on average by 200 nm. Typical AFM images after

391 etching are shown in **Figure 7a** and **Figure 7b**, taken for 1.15-μm-thick coalesced Ge grown at 700

392 °C (W_{window} = 0.66 μm and W_{mask} = 0.44 μm) and 2.67-μm-thick coalesced Ge grown at 650 °C

393 (W_{window} = 0.66 μm and W_{mask} = 0.34 μm). As a reference, the image of the 1.89-μm-thick blanket

394   Ge grown at 700 °C is shown in **Figure 7c**. The dark dots in the AFM images are etched pits
395   indicating the presence of TDs. The EPD values from **Figure 7a-7c** were obtained to be 7.0 x
396   10^7/cm^2, 7.9 x 10^7/cm^2, and 8.7 x 10^7/cm^2, respectively. Our previous reports showed that the
397   obtained EPDs in this etching condition are equal to TDDs determined by plan-view transmission
398   electron microscopy (TEM)[4,32–34]. The measured EPD of blanket Ge layer (7.9 ± 0.8 x 10^7/cm^2)
399   agrees well with TDD obtained from plan-view TEM observation with a relatively large area of 6
400   x 8 µm^2 (8.7 ± 0.2 x 10^7/cm^2), indicating that the EPD is equal to TDD.

402   In order to compare the experimentally obtained TDDs with calculations, take into account the
403   effect of thickness on TDD. There is a trend that TDD decreases as the Ge thickness increases
404   because of increased chances for the pair annihilation of TDs. Therefore, the reduction of TDD
405   observed for the coalesced Ge, thinner than blanket Ge, should be ascribed to the mechanism
406   described in **Figure 3 and Figure 4** (i.e., we need to calculate the normalized TDD to compare the
407   experimentally obtained TDDs with the calculated ones in **Figure 4**). Before the normalization, a
408   correction of TDD for blanket Ge ($\rho_{blanket}$) was performed, considering the thickness and the
409   growth temperature on TDD. Similar to the previous reports[35,36], $\rho_{blanket}$ [/cm^2] is approximately
410   expressed as 2.52 x 10^{13} x [d (nm)]$^{-1.57}$ for the Ge layers grown in the temperature range of 530–
411   650 °C using a UHV-CVD. Here, d is the thickness of the blanket Ge layer. $\rho_{blanket}$ [/cm^2] is reduced
412   for the Ge layers grown at 700 °C, and approximately expressed as 2.67 x 10^{12} x [d (nm)]$^{-1.37}$.

414   **Figure 7d** shows the normalized TDD as a function of APR, $W_{window}/(W_{window} + W_{mask})$. TDDs in
415   coalesced Ge grown at 650 °C are shown as blue triangles and those grown at 700 °C as red
416   diamonds. Since SEG Ge at 650 °C shows some wetting with the SiO$_2$ mask, the growth data
417   should fall in between the black and blue lines. SEG Ge at 700 °C should be on the red line. The
418   experimental results are in good agreement with the calculation based on the cross-sectional
419   shape and wetting conditions.

421   As described above, it is concluded that the behavior of TDs is well explained by the model based
422   on the image force of growth surfaces on TDs. In order to understand the interaction of TD with
423   the surface, we have observed TDs with a bright-field cross sectional STEM. A defect is observed
424   being bent and terminated on a surface of a semicylindrical void in **Figure 8a**. This behavior of
425   the TD is quite similar to calculated trajectories of TDs shown in **Figure 3**. However, the observed
426   trajectory of TD does not exactly reproduce the one we predicted in **Figure 3**. The difference
427   would be explained as the result of a TD transformation in order to minimize its energy during or
428   after the growth (e.g., temperature decrease from growth temperature to room temperature).
429   **Figure 8b** shows a simulation of strain in the coalesced Ge epilayer on Si. Tensile strain is induced
430   in the Ge layer on Si because of the mismatch of thermal expansion coefficient between Ge and
431   Si. The simulation indicates that strain accumulation occurs at the top of the semicylindrical voids
432   and strain relaxation at the sub-surface layer of the semicylindrical voids, which would motivate
433   TDs to transform.

435   On the other hand, **Figure 8c** shows defect generation at the top of a void, although the
436   generation point would be removed during the preparation of the TEM specimen. The defect in
437   **Figure 8c** is close to a straight line, but the angle between the defect and (001) plane (≈78.3°)

438   does not agree with that for the {111} plane (54.7°).

439

440   The electron diffraction pattern shown in **Figure 8d** was obtained near the defect in **Figure 8c**.
441   The absence of streak light indicates that there should not be a 2D structure (i.e., the defect is a
442   dislocation). In previous reports[28-31,37], 2D defects were formed showing clear a streak light in
443   electron diffraction patterns, which is against the one observed in the present work. The
444   observation results (the absence of 2D defects) supports the prediction that the voids and their
445   free surfaces contribute to release strain in Ge on Si, or otherwise cause the crystal
446   misorientations between adjacent SEG Ge layers. This is consistent with a previous report briefly
447   suggesting that the formation of 2D defects is prevented in coalesced SEG Ge layers with voids
448   on the SiO_2 masks[38].

449

450   There are two candidates for the TD generation shown in **Figure 10c**: the strain distribution and
451   the misorientation between SEG Ge layers. In epitaxial Ge on Si, the tensile strain is induced in
452   Ge due to the mismatch of thermal expansion coefficient between Ge and Si[39]. The simulation
453   result shown in **Figure 8b** indicates accumulation of tensile-strain (~0.5%) at the top of the void
454   as mentioned above. Such strain accumulation at the void top could result in TD generation
455   shown in **Figure 8c.** Another candidate, the misorientation between SEG Ge layers, has been
456   assumed to generate 2D defects as observed in previous reports showing coalescence of SEG Ge
457   layers[28–31,37]. In the present work, however, the generation of 2D defects would be suppressed
458   owing to the presence of voids as briefly mentioned in a previous report[38], but result in the TD
459   generation owing to imperfect suppression. More detailed discussion for the misorientation-
460   induced dislocation will be described in a later part with schematic illustrations (**Figure 12**).

461

462   **Figure 9a** and **Figure 9b** show bright-field plan-view TEM images of a coalesced Ge layer (W_{window}
463   = 0.82 µm, W_{mask} = 0.68 µm) and a blanket Ge layer, respectively, grown on the same substrate.
464   For the plan-view TEM observations, TEM specimens were formed using the top 200 nm regions
465   of the Ge layers as described in step 2.4.3 and are indicated by red dashed squares in the
466   schematic cross-sections at the top of **Figure 9.** SiO_2 mask stripes are aligned to the [110]
467   direction for the coalesced Ge in **Figure 9a.** The plan-view TEM image shown in **Figure 9a** was
468   taken for a 6 µm x 8 µm area. Although there are five pairs of SiO_2 masks and Si window areas in
469   this TEM image, the areas above the SiO_2 masks and Si windows are not distinguishable in the
470   TEM image. This is because the observed area (top 200 nm) is far above where semicylindrical
471   voids are located (bottom 150 nm).

472

473   It is found that TDDs obtained from **Figure 9a** and **Figure 9b** are 4.8 x 10^7/cm² and 8.8 x 10^7/cm²,
474   respectively. As shown in **Figure 7d**, EPD measurements reveal that TDD in the coalesced Ge layer
475   (W_{window} = 0.82 µm and W_{mask} = 0.68 µm) is 4 x 10^7 cm⁻². Thus, the TDD in **Figure 9a** shows a good
476   agreement with the EPD shown in **Figure 7**. It is also notable that neither EPD measurements nor
477   TEM observations show TDD re-increase, which is frequently shown when SEG Ge layers coalesce
478   (i.e., the TDD re-increase owing to generation of TDs (**Figure 8b**) is suppressed to such an extent
479   that the TDD re-increase is ignorable in the present TDD range (on the order of 10^7/cm²)).

480

481   It should be remarked that a TD-free area as large as 4 µm x 4 µm is realized in the coalesced Ge,

as in **Figure 9a**. Although the blanket Ge in **Figure 9b** shows TDs with a relatively uniform distribution, the coalesced Ge has high and low TDD areas. Such differences in TD distribution suggest that further TDD reduction would be achievable in the coalesced Ge. 1 TD in a 4 μm x 4 μm area, which is observed in **Figure 9a**, corresponds to TDD of 6.25 x 10^6/cm^2.

Comparing coalesced Ge (**Figure 9a**) and blanket Ge (**Figure 9b**), it is clear that the lengths of the defect lines in coalesced Ge are longer than those in blanket Ge. In coalesced Ge, there are typically 1-μm-long defect lines, and they are aligned to the [110] direction. Note that the [110] direction is the length direction of the SiO$_2$ stripes. There are two possible explanations for such long defect lines: (i) 2D defects are observed and (ii) dislocations are inclined in the [110] direction. However, 2D defects are immediately denied because of the widths of the observed long defects (i.e., 2D defects on {111} planes should show wider defect lines). Geometrically, 2D defects on the {111} planes should show 140-nm-wide defect lines, taking into account the thickness of the TEM specimen (200 nm) and the angle of the {111} with (001) planes (54.7°). The plan-view TEM image shows that the defect lines are 10–20 nm in width, which is much narrower than 140 nm. Thus, the defects shown as long lines should be ascribed to (ii) dislocations inclined in the [110] direction. A simple geometrical calculation gives the angle between the inclined dislocations and (001) planes: $\tan^{-1}$(200 nm/1 μm) = 11.3°. Note that, as shown in **Figure 8b**, TDs in blanket Ge tend to be directed almost vertical to the substrate if no post-growth annealing is performed, showing small black dots in plan-view TEM images.

For more detailed analysis of the inclined TDs, a small area with high-TDD is arbitrarily observed as in **Figure 10**. The TEM specimen was prepared from the top 200 nm of the coalesced Ge layer, the same as the plan-view TEM observations above.

Figure 10a and **Figure 10b** show dark-field (**g** = [220] for **Figure 12a** and [2$\bar{2}$0] for **Figure 12b**) plan-view TEM images taken at the same area. In **Figure 12**, four inclined dislocations were observed in a 4 μm x 4 μm area. **Figure 10b** reveals that one inclined dislocation (the red-circled one) disappears when diffraction vector **g** = [2$\bar{2}$0], which indicate that the Burgers vector is determined to be [110] or [1$\bar{1}$0] for the red-circled dislocation. Since the defect line is in the [110] direction, the dislocation is found to be a screw dislocation. The other three inclined dislocations (green-circled ones) are ascribed to the mixed dislocations because they did not disappear whatever diffraction vector **g** was chosen.

There are two possible explanations for the inclination of TDs in coalesced Ge layers: (i) Ge growth in [110] direction, and (ii) defect generation when SEG Ge layers coalesce.

Ge growth in [110] direction
Figure 11 shows a plan-view SEM image and the growth process to form a flat epitaxial layer from a non-planar SEG surface as a schematic movie. Reflecting the edge undulation of the SiO$_2$ stripe patterns formed by the EB lithography and wet chemical etching, the coalescence preferentially starts at some points, and then proceeds in the [110] and [$\bar{1}\bar{1}$0] directions above the SiO$_2$ masks. **Figure 11b** and **Figure 11c** schematically show the bird's eye view and the (1$\bar{1}$0) cross-sectional view when SEG Ge layers are partly coalesced. A TD generated at a growth window appears above

526   the void as shown in **Figure 3**, and then the TDs start to propagate in the [110] or [$\bar{1}\bar{1}0$] direction
527   due to the image force. This leads to TDs inclined in the [110] direction (as in **Figure 9a**). The red
528   solid line in **Figure 11c** shows a TD bent in the [110] direction according to the model above,
529   which explains the presence of the inclined TDs observed in **Figure 9a** and **Figure 10** on a
530   qualitative basis.

532   The mechanism can explain both edge and screw TDs, taking into account the Burgers vectors of
533   TDs generated at Ge/Si interfaces[40]. As Ge is grown on a Si substrate, edge misfit dislocations
534   (MDs) are formed to release strain, and MDs are aligned in the [110] or [$1\bar{1}0$] direction. The MDs
535   form threading segments (i.e., TDs), and the Burgers vectors for the TDs originated from MDs
536   aligned in the [110] direction (MD_{110}) are a/2[$1\bar{1}0$] or a/2[$\bar{1}10$] (a: the lattice constant). On the
537   other hand, the Burgers vectors are a/2[110] or a/2[$\bar{1}\bar{1}0$] for the TDs originated from MDs aligned
538   in the [$1\bar{1}0$] direction ($MD_{1\bar{1}0}$). In the case that the TDs from MD_{110} are inclined to the [110]
539   direction, plan-view TEM observations show the TDs as edge dislocations. Similarly, when the
540   TDs from $MD_{1\bar{1}0}$ are inclined to the [110] direction, they are observed as screw dislocations.

542   Defect generation when SEG Ge layers coalesce
543   **Figure 12** shows schematics explaining generation of defects when SEG Ge layers coalesce with
544   small rotation (i.e., misorientation). As schematically illustrated in **Figure 12**, the misorientation
545   should generate edge/screw/mixed dislocations at the coalescence interface. In **Figure 12**,
546   misorientation between two SEG Ge layers in the [110] direction is decomposed into three types
547   of rotations. **Figure 12a-12c** shows the rotation around the [110] axis, the [001] axis, and the
548   [$1\bar{1}0$] axis, respectively.

550   The coalescence in **Figure 12** is assumed to occur between a strictly epitaxial Ge layer (Ge (001))
551   and an adjacent SEG Ge layer with a misorientation (m-Ge). The rotation around the [110] axis
552   (**Figure 12a**) results in the generation of edge dislocations parallel to the [110] direction at the
553   boundary indicated as a dashed line. Similarly, as in **Figure 12b**, the edge dislocations parallel to
554   the [001] direction are generated as a result of the rotation around the [001] axis. On the other
555   hand, the rotation around the [$1\bar{1}0$] axis, shown in **Figure 12c**, generates a screw dislocation
556   network, which is composed by dislocations of **b** = [110] and **b** = [001], being similar to the case
557   for direct bonding of Si (001) surfaces showing screw dislocation network[41]. The screw TD
558   observed in **Figure 10** could be ascribed to the coalescence with misorientation of a rotation
559   around [$1\bar{1}0$] axis. The combination of rotations around [110] axis (**Figure 12a**) and around [$1\bar{1}0$]
560   axis (**Figure 12c**) can explain the mixed TDs shown in **Figure 12**. The mixed dislocation shown in
561   **Figure 9b** is also explained by the combination of the rotation around the [001] axis (**Figure 12b**)
562   and the rotation on the [$1\bar{1}0$] axis (**Figure 12c**).

564   Assuming that the dislocations originated from the misorientation are generated at a density of
565   1 x 10^7/cm^2, the average angle of the rotation around [$1\bar{1}0$] axis is estimated to be 0.034° [42].
566   Compared to the estimation, we have already reported that there are fluctuations of orientation
567   in a line-shaped SEG Ge layer for 100 arcsec (= 0.028°), employing micro-beam X-ray diffraction
568   observations[43]. The reported fluctuations of orientation and estimated rotation angle show good
569   agreement, which supports the TD generation mechanism based on misorientations.

570

571 **FIGURE AND TABLE LEGENDS:**

572

573 **Figure 1: Schematic illustrations of line-and-space shaped and 4 mm square SEG masks on a**
574 **Si(001) substrate.**

575

576 **Figure 2: Pictures for parts of an UHV-CVD machine; gas cabinet, process chamber, load lock**
577 **chamber, and operation computer.**

578

579 **Figure 3: Calculated trajectories of 4 TDs in (a) round-shaped SEG origin, aperture ratio = 0.8,**
580 **(b) round-shaped SEG origin, aperture ratio = 0.1, (c) {113}-facetted SEG origin, aperture ratio**
581 **=0.8, and (d) {113}-facetted SEG origin, aperture ratio = 0.1.**

582

583 **Figure 4: Calculated TDDs in coalesced Ge originated from {113}-facetted SEG Ge (blue line) and**
584 **round-shaped SEG Ge (red line).**

585

586 **Figure 5: Distribution maps and SEM images of coalesced/non-coalesced Ge layers.**

587

588 **Figure 6: (a) A cross-sectional HAADF STEM image of coalesced Ge (W_{window} = 0.66 μm, W_{mask} =**
589 **0.84 μm) grown at 700 °C with 10-nm-thick $Si_{0.3}Ge_{0.7}$ demarcation layers, and (b) a schematic**
590 **illustration corresponding to the conditions shown in (a).**

591

592 **Figure 7: Typical AFM images in order to measure EPDs for (a) 1.15-μm-thick coalesced Ge**
593 **grown at 700 °C (W_{window} = 0.66 μm and W_{mask} = 0.44 μm), (b) 2.67-μm-thick coalesced Ge grown**
594 **at 650 °C (W_{window} = 0.86 μm and W_{mask} = 0.34 μm), and (c) 1.89-μm-thick blanket Ge grown at**
595 **700 °C, and summary of the EPD measurement results in (d).**

596

597 **Figure 8: (110) cross-sectional (a) STEM and (b) TEM images of coalesced Ge layers (W_{window} =**
598 **0.66 μm and W_{mask} = 0.44 μm), (c) electron diffraction pattern obtained near the defect shown**
599 **in (b), and (d) finite element method simulation result of a strain distribution in the coalesced**
600 **Ge.** Figures 9(a), (c), and (d) have been modified from [20].

601

602 **Figure 9: Bright-field plan-view TEM images of (a) a coalesced Ge layer (W_{window} = 0.82 μm,**
603 **W_{mask} = 0.68 μm) and (b) a blanket Ge layer.**

604

605 **Figure 10: Plan-view TEM images of a high-TDD small area with g vectors of (a) [220] and (b)**
606 **[2$\bar{2}$0].** This figure has been modified from [20].

607

608 **Figure 11: (a) A plan-view SEM image, (b) a bird's eye schematic image, and (c) a (1$\bar{1}$0) cross-**
609 **sectional schematic image of a partially coalesced SEG Ge.** This figure has been modified from
610 [20].

611

612 **Figure 12: Schematics of defect generation when SEG Ge layers coalesce with crystal rotation**
613 **around (a) [110], (b) [001], and (c) [1$\bar{1}$0] orientation.** This figure has been modified from [20].

614
615 **Table 1: A summary of achieved TDD and drawbacks in view of photonic device application for**
616 **conventional/presented TDD reduction methods.**
617
618 **Supplemental Figure 1: Four typical methods widely employed to reduce TDD in epitaxial Ge**
619 **on Si: (a) thermal annealing, (b) SiGe graded buffer, (c) Aspect ratio trapping (ART), and (d) Si**
620 **pillar seeds.**
621
622 **Supplemental Video 1: Schematic illustrations of a TD bent owing to image force in a round-**
623 **shaped SEG Ge.**
624
625 **DISCUSSION:**
626 In the present work, TDD of $4 \times 10^7/cm^2$ were experimentally shown. For further TDD reduction,
627 there are mainly 2 critical steps within the protocol: SEG mask preparation and epitaxial Ge
628 growth.
629
630 Our model shown in **Figure 4** indicates that TDD can be reduced lower than $10^7/cm^2$ in coalesced
631 Ge when APR, $W_{window}/(W_{window} + W_{mask})$, is as small as 0.1. Toward further TDD reduction, SEG
632 masks with smaller APR should be prepared. As mentioned in step 2.1.2, the minimum values of
633 W_{window} and W_{mask} were 0.5 μm and 0.3 μm, respectively, limited by the resolution in the
634 employed EB lithography system. One simple method to reduce APR is to modify lithography and
635 etching processes (e.g., to use another photoresist, to use better lithography system, to use
636 thinner SiO_2 layers with shallower BHF etching, etc.). Mature lithography and etching process will
637 enable SEG masks narrower than 100 nm. In the present work, coalesced Ge with a flat top
638 surface were obtained when $W_{mask} \leq 1$ μm. Thus, W_{window} of 100 nm and W_{mask} of 900 nm (APR =
639 0.1) will give us coalesced Ge with flat top surface in the present growth conditions.
640
641 In addition to that, the modification of SEG mask preparation should bring less edge undulation
642 of SEG masks, resulting in suppression of misorientation between Ge SEG layers. The TD
643 generation when SEG Ge layers coalesce (**Figure 11**) will be suppressed as the result of the
644 modification of SEG mask preparation.
645
646 As revealed by calculation results (**Figure 3**), suppression of Ge growth on SiO_2 is required to
647 reduce TDD. The suppression of Ge growth on SiO_2 is brought by modification of Ge growth step
648 (i.e., elevation of growth temperature, rotation of SEG mask, introduction of H_2 gas, and
649 reduction of the pressure of GeH_4 gas[44,45]).
650
651 The TDD reduction method proposed/verified in the present work is superior to existing methods
652 in terms of application for Ge photonic devices (i.e., TDD is reduced without any thermal
653 annealing nor thick buffer layers). The maximum process temperature was 700 °C, which is the
654 growth temperature, and the height of the void was ≈150 nm. Compared with existing methods,
655 the maximum temperature is lower than annealing temperature (typically 900 °C)[7], and height
656 of the void is shallower than SiGe graded buffer layers (typically several μm)[10], SiO_2 trenches for
657 ART (typically 0.5–1 μm)[13], and buffer layer for Ge growth on Si pillars (typically ≈5 μm)[18]. The

658   comparison of conventional/presented methods are summarized in **Table 1**.
659
660   Considering the footprint of a typical Ge photonic device ($\approx$100 μm^2), TDD lower than 10^6/cm^2,
661   and a number of TD < 1/device will be the final goal. Since the theoretical limit of TDD for this
662   method is 0, TDD lower than 10^6/cm^2 is potentially achievable. Toward the goal, more optimized
663   lithography and etching will be investigated.
664

671

672   **DISCLOSURES:**
673   The authors have nothing to disclose.
674

675   **REFERENCES:**
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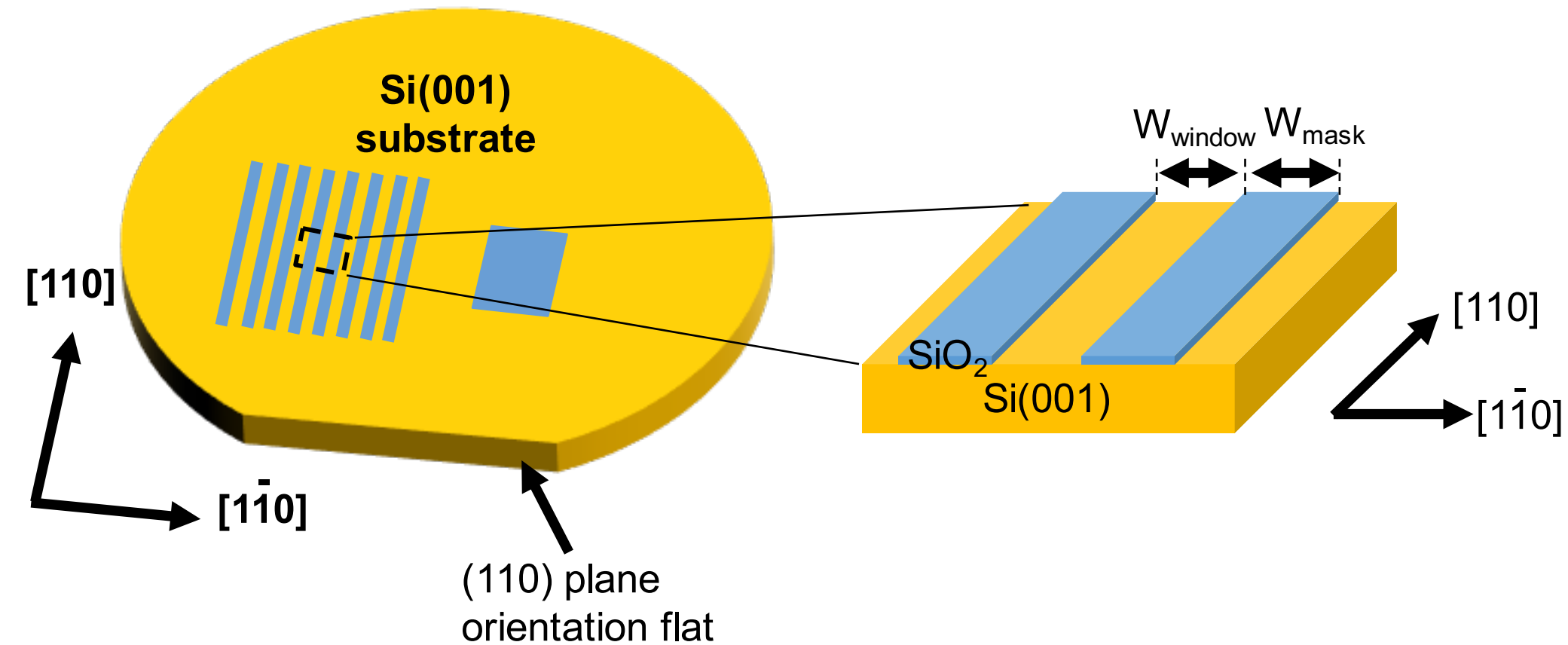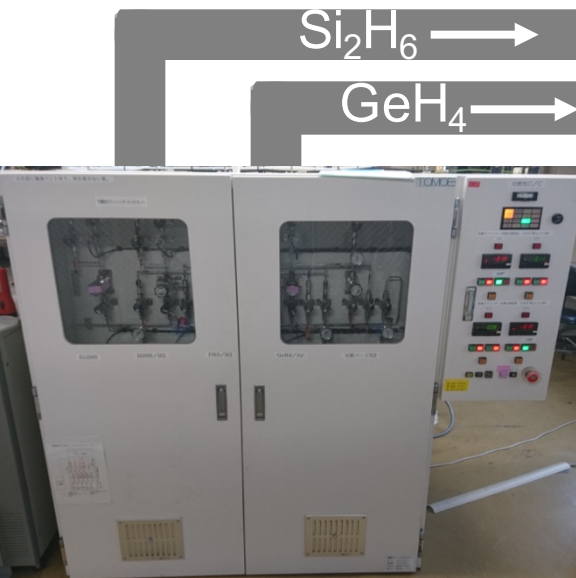783   **15** (2), 1–9 (2014).

784

Figure 1　　　　　　　　　　　　　　　　　　　　Click here to access/download;Figure;Figure1.pdf

Figure 1

Figure 2

$Si_2H_6 \rightarrow$

$GeH_4 \rightarrow$

Gas cabinet

Growth chamber

Load lock chamber

Operation panel

Figure 3

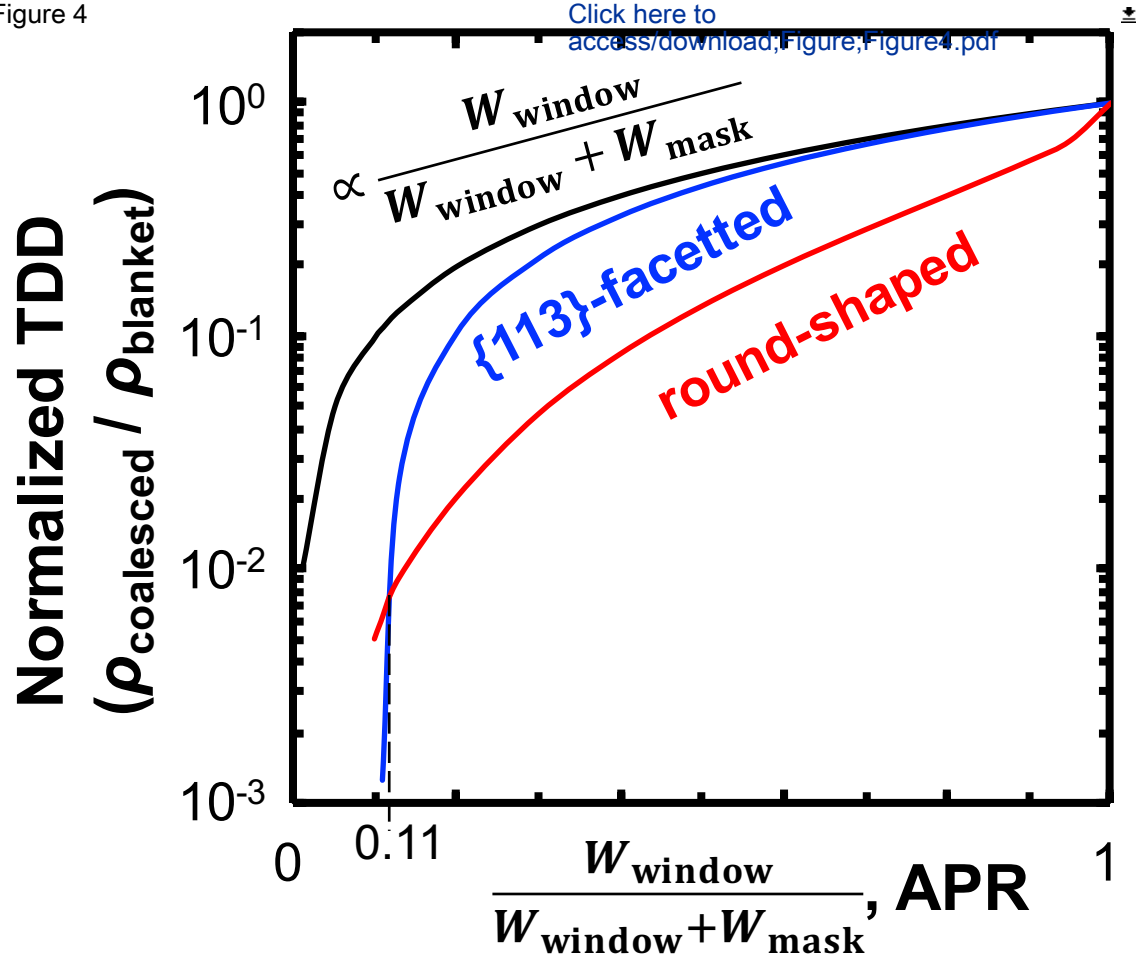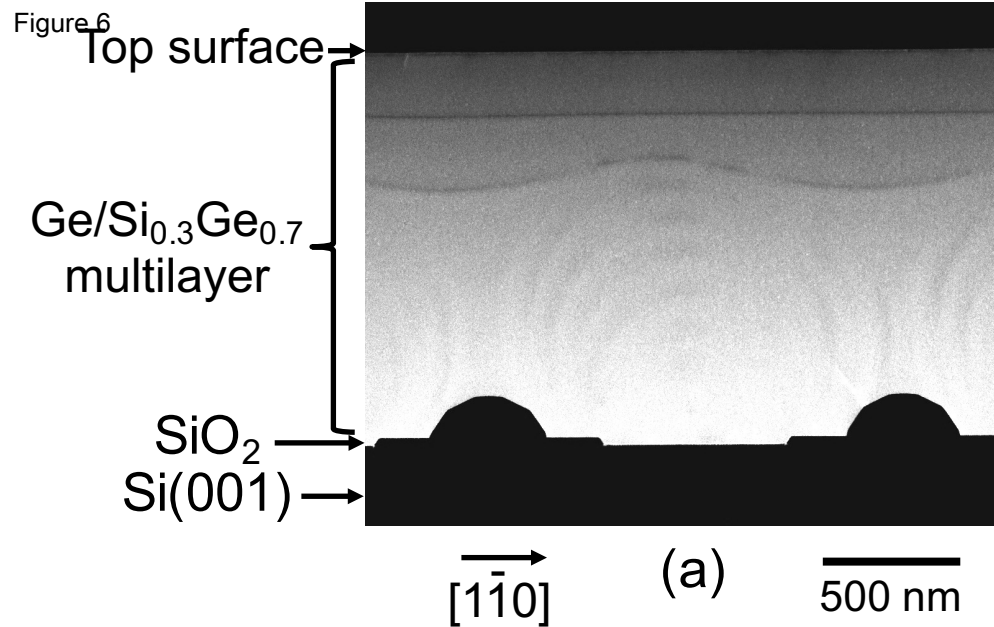| Original SEG cross-section	Aperture ratio		
	0.8	**0.1**	**0.1 (Ge on SiO₂)**
Round-shaped	(a)	(c)	(e)
{113}-facetted	(b)	(d)	(f)

Figure 4

Figure 5

(a) 700 ˚C

(b) W_{window} = 0.96 µm, W_{mask} = 1.84 µm

(c) W_{window} = 1.06 µm, W_{mask} = 0.84 µm

(d) W_{window} = 0.86 µm, W_{mask} = 0.54 µm

(e) 650 ˚C

(f) W_{window} = 0.86 µm, W_{mask} = 1.84 µm

Figure 6

(a) Top surface — Ge/Si$_{0.3}$Ge$_{0.7}$ multilayer — SiO$_2$ — Si(001), [1$\bar{1}$0], 500 nm

(b) Top surface — Ge/Si$_{0.3}$Ge$_{0.7}$ multilayer — SiO$_2$ — Si(001), [1$\bar{1}$0]

Figure 7

W_{window} = 0.66 µm
W_{mask} = 0.44 µm
700 ˚C (round-shaped)
1.15-µm-thick

W_{window} = 0.66 µm
W_{mask} = 0.34 µm
650 ˚C ({113}-facetted)
2.67-µm-thick

Blanket Ge
700 ˚C
1.89-µm-thick

(a) 2 µm   (b) 2 µm   (c) 2 µm

(d)

Normalized TDD ($\rho_{coalesced}$ / $\rho_{blanket}$)

$\propto \dfrac{W_{window}}{W_{window} + W_{mask}}$

{113}-facetted

Round-shaped

650 ˚C

700 ˚C

$\dfrac{W_{window}}{W_{window}+W_{mask}}$, APR

Figure 8

Ge

Si (001)

[1$\bar{1}$0]

(a)

500 nm

Ge

Si (001)

(c)

500 nm

+0.50 %

+0.24 %

0 %

Ge

Si

(b)

(004)   (2$\bar{2}$0)

(d)

Figure 9

(a)

(b)

Figure 10

Direction of SiO$_2$ mask stripes

g = [220]

g = [2$\bar{2}$0]

(a)

(b)

1 µm

1 µm

Figure 12

(a)

Twin Boundary

[001]

[110]

[1̄10]

[001]

[1̄10]

Ge (001)

m-Ge

Ge (001)

Si (001)

Ge (001)

m-Ge

(b)

Twin Boundary

[001]

[110]

[1̄10]

[110]

[1̄10]

Ge (001)

m-Ge

Ge (001)

Si (001)

Ge (001)

m-Ge

(c)

[001]

[110]

[1̄10]

[001]

[110]

Ge (001)

m-Ge

Ge (001)

Si (001)

m-Ge over Ge (001) Screw Dislocation

b
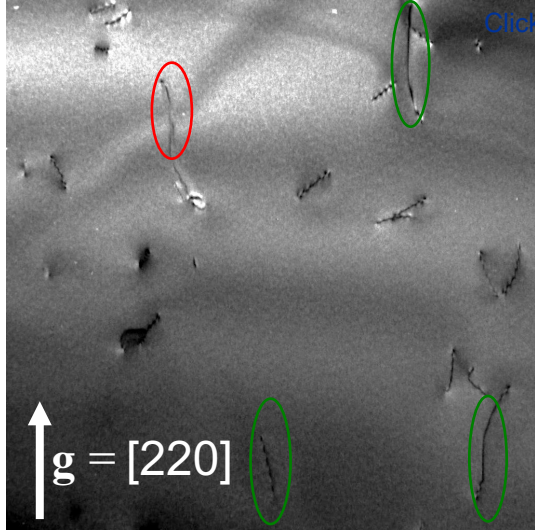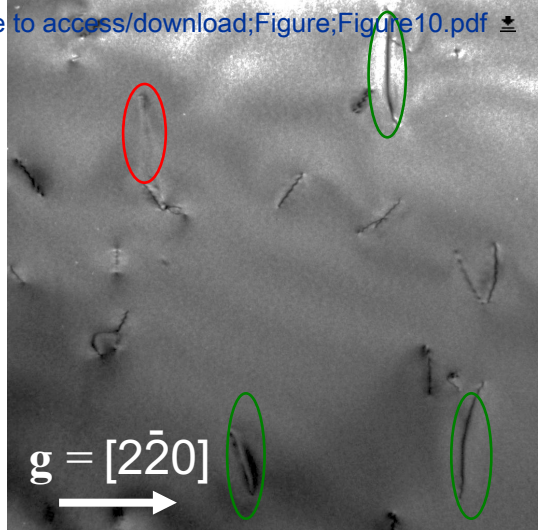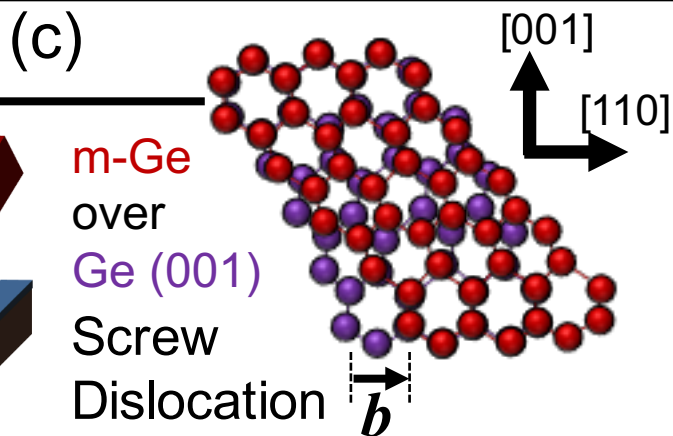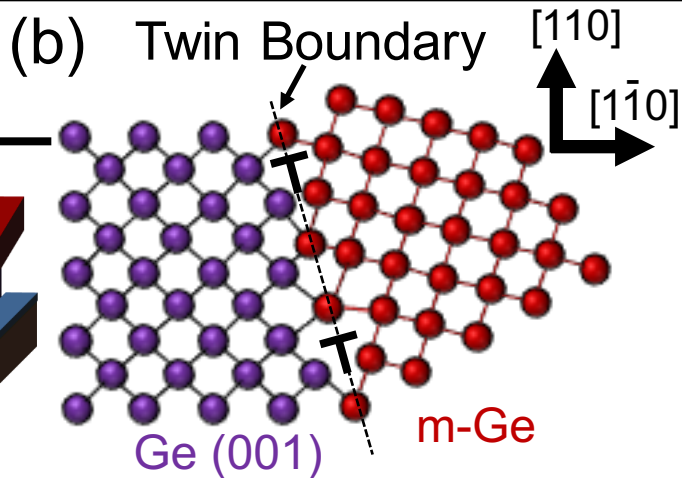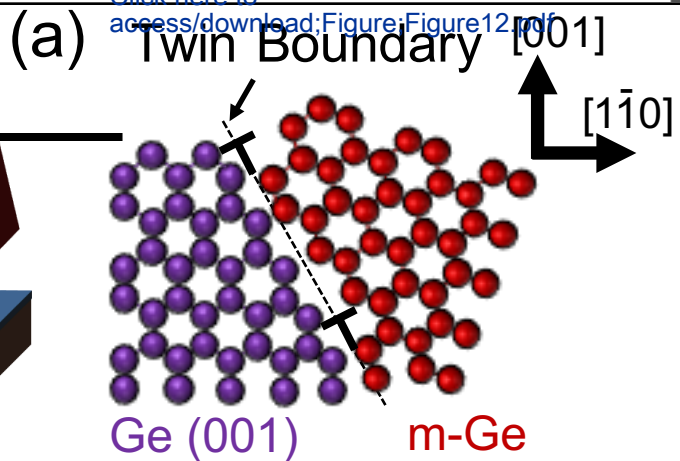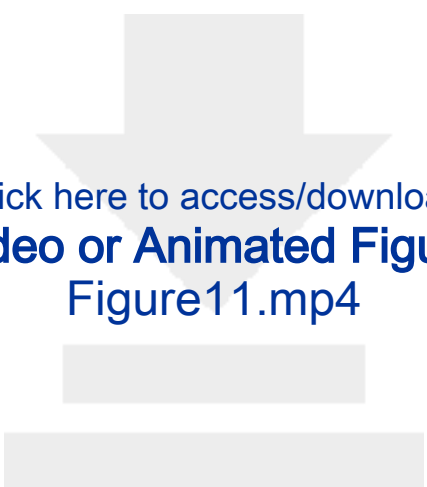
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Table 1

Method	Achieved TDD (cm−2)	Temperature (°C)
Thermal annealing	2e7	≈900 °C
SiGe graded buffer	1e6	growth temperature (600−700 °C)
ART	1e6	growth temperature (600−700 °C)
Si pillar seeds	1e5	≈800 °C
This work	4e7	growth temperature (700 °C)

Buffer layer thickness
≈100 nm (low-temperature buffer)
2–3 μm
500–1000 nm
≈5 μm
≈150 nm

Name of Material/ Equipment	Company	Catalog Number	Comments/Description
AFM	SII NanoTechnology	SPI-3800N	
BHF	DAIKIN	BHF-63U	
CAD design	AUTODESK	AutoCAD 2013	Software
CH_3COOH	Kanto-Kagaku	Acetic Acid	for Electronics
CVD	Canon ANELVA	I-2100 SRE	
Developer	ZEON	ZED	
Developer rinse	ZEON	ZMD	
EB writer	ADVANTEST	F5112+VD01	
Furnace	Koyo Thermo System	KTF-050N-PA	
HF, 0.5 %	Kanto-Kagaku	0.5 % HF	
HF, 50 %	Kanto-Kagaku	50 % HF	
HNO_3, 61 %	Kanto-Kagaku	HNO3 1.38	for Electronics
I_2	Kanto-Kagaku	Iodine 100g	
Photoresist	ZEON	ZEP520A	
Photoresist remover	Tokyo Ohka	Hakuri-104	
Surfactant	Tokyo Ohka	OAP	
TEM	JEOL	JEM-2010HC	

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CORRESPONDING AUTHOR

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Title: Visiting Professor and Emeritus Professor

Signature: *Kaz Wada*   Date: *Nov. 21, '18*

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Reply to the Reviewer

We would like to thank the reviewers for their fruitful comments. Since Reviewer #1 and #2 suggests that the original manuscript is suitable for publication, we would like to answer Reviewer #3's comments. Considering their comments, we have revised the manuscript and prepared a manuscript for reviewers with highlight. In the revised manuscript for review, the revised/added descriptions are highlighted by BLUE characters.

Reviewer #3
[General Comment]
The authors suggest a method of dislocation reduction in Ge epitaxial layers with semicylindrical voids on Si. they suggest a theoretical calculation and experimental verification
I suggest to give the manuscript back to the authors in order to revise it:
Major Concerns:
We are assessing a manuscript for the production of a movie, so the following things are disturbing the reviewers assessment "ab initio"

[Comment 1]
The manuscript - 34 pages - in the present shape is hard to assess since many figures are presented
(a) at the end of the manuscript
(b) not enumerated in their original order
(c) without captions
You cannot jump back and forth in a movie either....

[Reply 1]
We have prepared a manuscript for reviewer, which is modified for easy reading.
Here, we put the figures where they are mentioned.
We are afraid there were some mistakes in uploading the movies in the last submission.
We believe now you can jump back and forth in the movies.

[Comment 2]
The intro of the manuscript proposal lacks the definition of clear merits; the "eye catcher" is missing

[Reply 2]
We have added a sentence to mention the merit of this method at the end of INTRODUCTION part (lines 98–100) and in DISCUSSION PART (lines 585–593).
The merit of the proposed method is that dislocations are removed without any thermal annealing or thick buffer layers.
Conventional methods have been employed thermal annealing or thick buffer layer as

1

mentioned in lines 67–81 in INTRODUCION and Table 1 in DISCUSSION.

[Comment 3]
The subject of presented work should profit from the presentation as a movie as compared as to be published as a methods paper in some materials journal or applied physics journal
    So.. I am missing in the presentation of the manuscript any initial trial
    (a) of presenting the procedure in the laboratory
    (b) of presenting something "dynamical" which is
    (*) interesting enough to be directly followed by the consumers eye
    (*) which is easy enough to be understood at first or second sight
    I do not see the sense of the animated figures as such, without a direct and immediate counterpart as the demonstration in situ would be.

[Reply 3]
We have revised the PROTOCOL part in order to show more details of experimental procedure.
    The revised PROTOCOL part shows detailed procedure in the laboratory so that anyone can understand/reproduce the experiments.

[Comment 4]
The manuscript so far lacks in one sense coherence:
    A movie should be interesting for an increased auditorium; it should be understandable for deaf as well as for blind people with some efforts! It should also be interesting for non-experts such as students in the advanced classes

[Reply 4]
As the reviewer pointed out, this manuscript would be somehow difficult to understand for non-experts because the presented method employs a new mechanism (image force) to reduce TDD in Ge: even experts of Ge growth on Si are not familiar with image force.
    However, the basic idea, TDs are bent to be normal to growth surface, is so simple that everyone can understand what happens in Ge if one can understand geometrical structure.
    Thus, we have added schematic illustrations (Fig. 3 in the revised manuscript) in order to help understanding of geometrical structure of SEG masks.

[Comment 5]
A method publishing manuscript must be assessible for reproduction

[Reply 5]
We have revised PROTOCOL part in order to show more details of experimental procedure.

[Comment 6]
A method publishing manuscript must be embedded in the research background as the reader, or the auditorium must see bright and clear why it should be an advantage to use the method,

compared to others, what is the improvement, bright and clear in figures words and numbers.

The manuscript should start with this as an intro and it should praise the merits again in the discussion.

[Reply 6]
We have added a description showing the advantage of this method at the end of INTRODUCTION part (lines 98–100) and in DISCUSSION PART (lines 585–593).

In DISCUSSION part, we have added a table showing the summary of conventional/presented TDD reduction methods in order to make the advantage of the presented method clear.

[Comment 7]
The geometry aspects of this manuscript:

This aspect naturally includes many aspects where the crystal geometry plays a role and the application of geometrical, spacial techniques. My personal spacial sense is beyond doubt above average in the community of physicists and christallographers. If I need to read a technical passage many times, or if I have to repeat an animated figure a few times, and I still do not see their claimed to be key feature, it will not appeal to the broad mass of material scientists and in needs to be improved.

Actually so far I do not see these points presented well in this manuscript. For these reasons I suggest to give the manuscript back for revision to the authors.

[Reply 7]
Although we would not fully understand exact meaning of your comment, we have regarded your "Comment 7" that our previous manuscript was not so clear and it was difficult to understand geometrical structure.

In order to help geometrical understanding, we have added a figure (Fig. 3 in the revised manuscript) showing schematic illustrations of SEG masks on a Si(001) substrate.

We believe that everybody sees Fig. 3 can understand the geometrical structure of SEG masks used in the present work, and we could answer your "Comment 7".

Rebuttal Letter

Title: A method of dislocation reduction in Ge epitaxial layers with semicylindrical voids on Si: theoretical calculation and experimental verification
Submission number: JoVE58897

Dear Dr. Vineeta Bajaj,
Review Editor of JoVE,

We are grateful to submit our manuscript to JoVE, entitled "A method of dislocation reduction in Ge epitaxial layers with semicylindrical voids on Si: theoretical calculation and experimental verification."
We have revised our manuscript in response to your comments as follows.

[Comment]
Parts of the manuscript have significant textual overlap with previous publication(s), including, possibly, the authors' own. All text must be original. Please see the attached iThenticate report and revise the following: 175-193, 199-206, 208-213, 215-224, 298-300, 304-310, 324-328, 341-344, 348-358, 360-367.

[Reply]
We have thoroughly revised the parts of the manuscript you pointed out.
The text in the revised manuscript should have no overlap with previous publications.

[Comment]
The protocol is not written as per the journal's style. Please format the manuscript accordingly. Attaching the authors instruction for your consideration.
The Protocol should be made up almost entirely of discrete steps without large paragraphs of text.
The Protocol should contain only action items that direct the reader to do something. Please number the Protocol to follow the JoVE Instructions for Authors. For example, 1 should be followed by 1.1 and then 1.1.1 and 1.1.2 if necessary.

[Reply]
We have revised the Protocol section to follow the JoVE Instruction for Authors.
Now the Protocol is made up of section 1 (1.1–1.4) and 2 (2.1.1–2.4.4).

[Comment]
Please ensure that all text in the protocol section is written in the imperative tense as if telling someone how to do the technique (e.g., "Do this," "Ensure that," etc.). The actions should be described in the imperative tense in complete sentences wherever possible. Avoid usage of phrases such as "could be," "should be," and "would be" throughout the Protocol. Any text that cannot be written in the imperative tense may be added as a "Note."

However, notes should be concise and used sparingly. Please include all safety procedures.

[Reply]
We have revised the Protocol, and now all sentences in the revised Protocol section are written in the imperative tense.
In addition, the Protocol has been revised not to use could/should/would.

[Comment]
Please highlight 2.75 pages or less of the Protocol (including headings and spacing) that identifies the essential steps of the protocol for the video, i.e., the steps that should be visualized to tell the most cohesive story of the Protocol. The highlighted steps should form a cohesive narrative with a logical flow from one highlighted step to the next. Remember that non-highlighted Protocol steps will remain in the manuscript, and therefore will still be available to the reader.

[Reply]
Since our protocol is less than 2.75 pages (almost 2 pages), we did not highlight the manuscript.
We hope all sentences in Protocol will be shown in video because all steps are essential to our experiments.

[Comment]
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[Reply]
We obtained permission to re-use the Figures from our previous publication, *IEEE J. Sel. Top. Quant. Elect.*, 24-6, 8201007, 2018.
We have added the citation in the corresponding Figure legends (Figs. 9, 11, 12, and13).

[Comment]
As we are a methods journal, please revise the Discussion to explicitly cover the following in detail in 3-6 paragraphs with citations:
a) Critical steps within the protocol
b) Any modifications and troubleshooting of the technique
c) Any limitations of the technique
d) The significance with respect to existing methods
e) Any future applications of the technique

[Reply]
We have revised Discussion part to cover a)–e) above.

The revised Discussion is made up of 3 parts; (A), (B), and (C).
(A) describes possible ways for further reduction of TDDs, corresponding to a), c), and e)
(B) describes possible ways to avoid Ge growth on SiO_2, corresponding to b) and c) and,
(C) describes suppression of TD generation when SEG Ge layers coalesce, corresponding to b).

Thank you again for your kind support and consideration on our submission to JoVE.

Sincerely,

Motoki Yako

Ph.D. candidate
Department of Materials Engineering
University of Tokyo

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[20] Yako, M., Ishikawa, Y., Abe, E., Wada, K., Defects and Their Reduction in Ge Selective Epitaxy and Coalescence Layer on Si With Semicylindrical Voids on SiO_2 Masks, *IEEE Journal of Selected Topics in Quantum Electronics*, 24 (6), 8201007 (2018).

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Title of the article	A method of dislocation reduction in Ge epitaxial layers with semicylindrical voids on Si: theoretical calculation and experimental verification
Publication the new article is in	Journal of Visualized Experiments
Publisher of the article	JoVE
Author of new article	Motoki Yako, Yasuhiko Ishikawa, Eiji Abe, and Kazumi Wada

Expected publication date	Mar 2019
Estimated size of the article (pages)	10
Requestor Location	The University of Tokyo Rm. 334, Eng. Bldg. 4 7-3-1, Hongo Bunkyo-ku, Tokyo 113-8656 Japan Attn: The University of Tokyo
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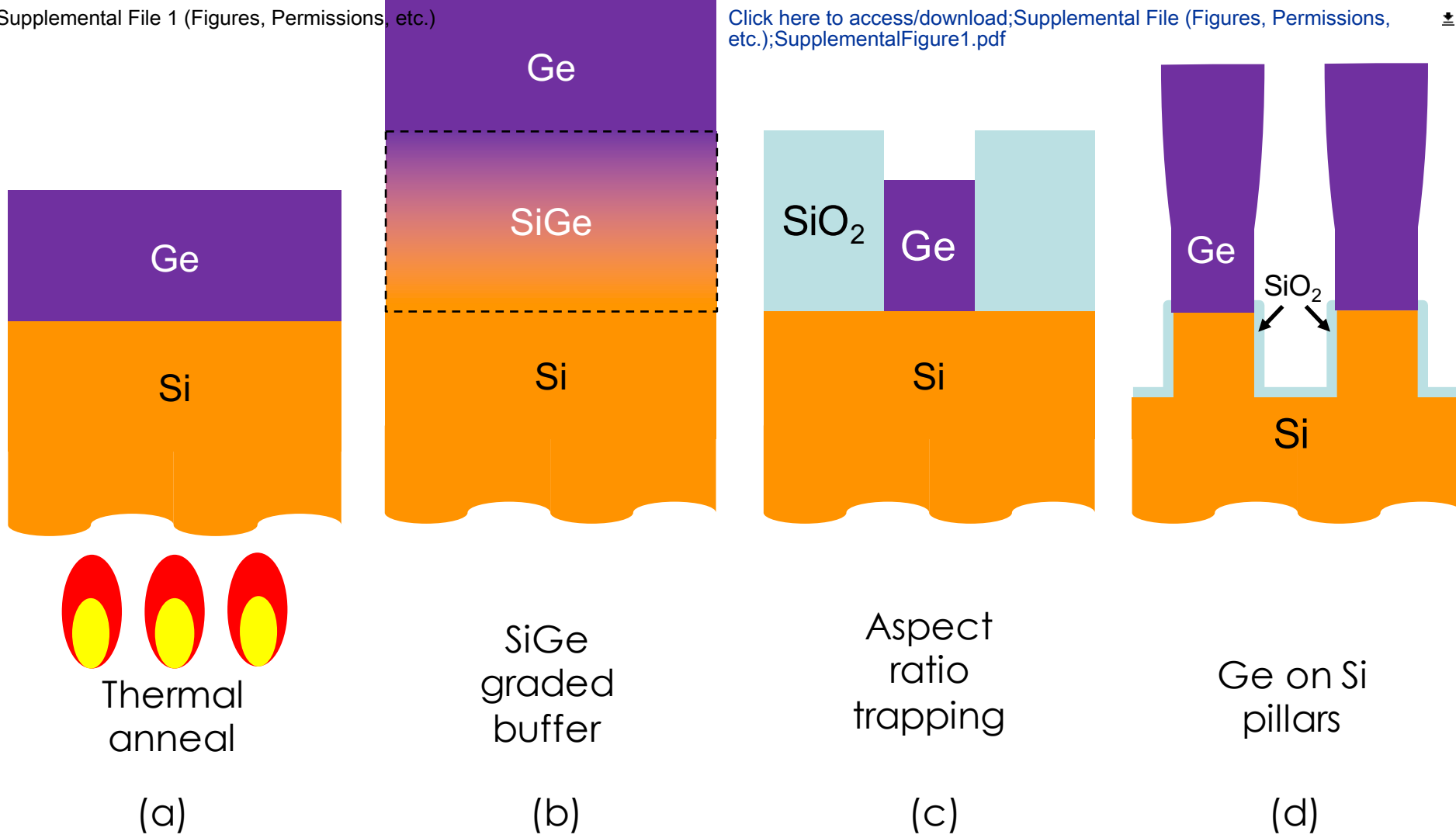
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(a) Thermal anneal

(b) SiGe graded buffer

(c) Aspect ratio trapping

(d) Ge on Si pillars

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