Journal of Visualized Experiments

Indium Phosphide Synaptic Device on Silicon to Emulate Synaptic Behavior for Neuromorphic Computing

--Manuscript Draft--

Article Type:	Invited Methods Article - JoVE Produced Video
Manuscript Number:	JoVE58657R2
Full Title:	Indium Phosphide Synaptic Device on Silicon to Emulate Synaptic Behavior for Neuromorphic Computing
Keywords:	Indium phosphide; field effect transistor; templated liquid-phase growth; synaptic device; neuromorphic computing; plasticity; metaplasticity; STDP
Corresponding Author:	Rehan Kapadia University of Southern California Los Angeles, California UNITED STATES
Corresponding Author's Institution:	University of Southern California
Corresponding Author E-Mail:	rkapadia@usc.edu
Order of Authors:	Debarghya Sarkar
	Jun Tao
	Wei Wang
	Qingfeng Lin
	Matthew Yeung
	Chenhao Ren
	Rehan Kapadia
Additional Information:	
Question	**Response**
Please indicate whether this article will be Standard Access or Open Access.	Standard Access (US$2,400)
Please indicate the **city, state/province, and country** where this article will be **filmed**. Please do not use abbreviations.	Los Angeles, California, USA

TITLE:

Indium Phosphide Synaptic Device on Silicon to Emulate Synaptic Behavior for Neuromorphic Computing

AUTHORS AND AFFILIATIONS:

Debarghya Sarkar[1] *, Jun Tao[1] *, Wei Wang[1], Qingfeng Lin[1], Matthew Yeung[1], Chenhao Ren[1], Rehan Kapadia[1]

[1]Ming Hsieh Department of Electrical Engineering, University of Southern California, Los Angeles, CA, USA

* These authors contributed equally.

Corresponding Author:

Rehan Kapadia (rkapadia@usc.edu)
Tel: (213)-821-0845

E-mail Addresses of the Co-authors:

Debarghya Sarkar (dsarkar@usc.edu)
Jun Tao (juntao@usc.edu)
Wei Wang (wang890@usc.edu)
Qingfeng Lin (qflin007@gmail.com)
Matthew Yeung (matthewdyeung@gmail.com)
Chenhao Ren (chenhaor@usc.edu)

KEYWORDS:

Indium phosphide, field effect transistor, templated liquid-phase growth, synaptic device, neuromorphic computing, plasticity, metaplasticity, STDP

SUMMARY:

The protocol describes the fabrication method of a scalable array of indium phosphide channel field-effect transistors from indium phosphide nanostripes grown directly on an Si/SiO_2 substrate with a thin MoO_x buffer and the characterization of the field-effect transistors as artificial synaptic devices.

ABSTRACT:

The protocol presented here describes, in detail, the process flow for a templated liquid-phase growth of crystalline indium phosphide (InP) nanostripes directly on an Si/SiO_2 substrate with MoO_x as a thin buffer layer. These InP nanostripes are, then, taken to fabricate InP channel field-effect transistors (FETs) in a scalable manner. Notably, this process allows researchers to obtain InP stripes in the exact geometry and location as may be required for scalable device array fabrication. Further, these FETs are utilized to demonstrate artificial synaptic behavior. The occupation of charge traps in the oxide is modulated by applying gate pulses that mimic pre-synaptic action potentials. The variation of the trapped charge density due to the time-correlated

activity of the pre- and postsynaptic neurons results in a threshold voltage shift leading to a change in channel conductance, which is interpreted here as the synaptic weight. A temporal variation of the threshold voltage shift and, thus, of the synaptic weight, arises from the relaxation of traps. Utilizing the time and neuronal activity-dependent synaptic weight change, several important non-linear biological synaptic behaviors are mimicked by the artificial synapse.

INTRODUCTION:

Currently, a wealth of research and development is taking place for the realization of a time-, energy-, and space-efficient computation for artificial intelligence applications[1]. Multiple hardware implementations of electrical circuits composed of elements and connectivity inspired by relevant components of the human brain are being developed toward realizing this paradigm, which is broadly referred to as neuromorphic computing. A widely accepted abstraction of the human brain for neuromorphic computing consists of neurons as logic units interleaved with synapses as specialized memory links. While neuron and synapse blocks have already been realized by multiple bilevel CMOS logic transistors and capacitors[2-16], the next generation circuits will potentially have single-device realizations for each of the neurons and the synapses.

A synapse[17] is a 20- to 40-nm junction between two neurons which aids in the communication of signals between the neurons. The strength of the synapse (better known as its 'weight') determines the amplitude of the current in the postsynaptic neuron generated because of the spiking activity in the presynaptic neuron. These weights are not hard-coded but evolve with time and activity[18]. The non-zero change in the synaptic weight after a neuronal activity is called plasticity and is a measure of the memory retention capacity of the synapse. The synaptic plasticity is, therefore, indicative of the prior neuronal activities and also of the degree to which future neuronal activities would be transduced. Future neuronal activities lead to further synaptic weight change. For the same neuronal activity, the plasticity of the synapse depends on the pre-existing weight of the synapse itself, a phenomenon referred to as metaplasticity[19,20]. Some of the other important weight-updating protocols of the synapse are spike number-dependent plasticity[21] and spike-timing-dependent plasticity (STDP)[22-26]. In spike number-dependent plasticity, the synaptic weight is a function of the number of action potentials arriving at the synapse simultaneously, while STDP demonstrates the synaptic weight change arising from time-correlated activity of the pre- and postsynaptic neurons.

So far, there are few reports on single-device neuron implementation[27,28], whereas single-device synapse implementation has found widespread attention[29,30]. Different material families and device architectures have been studied. Transistors based on controlling the population of charge traps in a floating gate[31] or intrinsically present at the interface or the bulk of the gate dielectric or semiconductor have been demonstrated[21,32-35]. Several classes of memristive[36] devices based on phase-change[37], and ferroelectric[38,39], ferromagnetic[28], and nanoionic[19,20,40-55] materials have also been implemented.

In order for neuromorphic computing to be truly ubiquitous while retaining high performance, technologies that would allow a scalable three-dimensional (3-D) integration of high-quality crystalline materials on different substrates are needed. The present 3-D integration approaches

are usually based on nanotube networks[56-59] or nanocrystalline channels[33,37] having low mobility or epitaxial growth, and transfer processes[21,34] having scalability issues. Templated liquid-phase growth is a technique that has been shown to produce large-area, single-crystal compound semiconductor materials on arbitrary, amorphous substrates and in a predesigned location and geometry[60-66]. In this work, we describe the protocol for the direct growth of a crystalline InP channel on a Si/SiO_2 wafer, and the realization of a scalable and potentially Si back-end-compatible array of artificial synapses based on an InP channel FET.

The protocol elaborated herein describes the step-by-step process of fabricating an array of InP nanostripe FETs on an Si/SiO_2 substrate and characterizing them as artificial synapses, a representative result which has been published recently[64].

PROTOCOL:

1. Scalable InP Nanostripe FET Fabrication on an Si/SiO_2 Substrate

1.1. Preparation of an Si/SiO_2 substrate

1.1.1. Soak an Si/SiO_2 substrate of 1 x 1 cm^2 sequentially in acetone, isopropyl alcohol, and deionized water for about 30 s each and dry the substrate by blowing N_2 on it.

1.1.2. Clean the substrate by O_2 plasma for a complete removal of organic substances on its surface.

Note: A 30-s plasma clean with 140 mTorr of O_2 pressure and 30 W of forward power is typically used.

1.1.3. Immediately proceed to step 1.2 or store the substrate in a vacuum desiccator.

1.2. InP nanostripe FET pattern lithography

1.2.1. Spin coat the substrate with lift-off resist (LOR) and perform a pre-exposure bake. For this, spread the LOR at 500 rpm for 5 s and, then, spin coat at 3,000 rpm for 60 s, and pre-exposure bake for 5 min at 175 °C.

1.2.2. Spin coat the substrate with photoresist (PR) and perform a pre-exposure bake. For this (typical process condition), spread the PR at 500 rpm for 5 s and, then, spin coat at 3,000 rpm for 60 s, and pre-exposure bake for 1 min at 110 °C.

1.2.3. Expose the photoresist to ultraviolet light through a contact mask to transfer the nanostripe pattern to the substrate. A typical exposure condition would be a flux of 5 mW/cm^2 for 18 s.

Note: Rectangular stripes of 2 µm in width were used in this study. This is a limitation by photolithography resolution, and smaller widths can be used if electron beam lithography is performed. Larger widths may also be used to increase the current drive if needed.

1.2.4. Develop the pattern-exposed resist by soaking the substrate in MF-319 developer for 150 s. Rinse it with deionized water and dry it by blowing N_2.

1.3. MoO_x/In deposition

1.3.1. Attach the patterned substrate to the sample stage of the evaporator using polyimide (*e.g.*, Kapton) tape (which has the capability of being cryogenically cooled by heat exchange with liquid nitrogen).

1.3.2. Pump down the chamber to base pressure (typically, 1 to 2 x 10^{-7} Torr). Bring the sample stage to cryogenic temperatures (-150 to -180 °C); for this, either directly flow liquid nitrogen through the stage or flow dry nitrogen cooled in a liquid nitrogen heat exchanger.

1.3.3. Evaporate 5 nm of molybdenum oxide (MoO_3, 99.9995%) at ~0.5 Å/s. Evaporate 100 nm of indium (In, 99.99995%) at ~4 Å/s (*in situ* with molybdenum oxide or separately).

Note: If a thermal evaporator is used, such as is done in the present work, alumina-coated molybdenum or tungsten boat may be used in both cases. In the thermal evaporator, a current through the boat is raised to achieve the required evaporation rates observed in the crystal monitor.

1.4. Deposit Capping SiO_2

1.4.1. Attach the MoO_x/In-deposited, patterned substrate to the stage of an e-beam evaporator using polyimide tape.

1.4.2. Pump down the chamber to base pressure (typically, 1 x 10^{-6} Torr). Evaporate 100 nm of SiO_2 (99.99%) at ~4 Å/s.

Note: If an e-beam evaporator is used, as is done in the present work, the high voltage and gun control are engaged and the rate is observed in the crystal monitor to perform the evaporation.

1.5. Transform the In film into InP by a templated liquid phase (TLP) approach

1.5.1. Immerse the sample in a suitable resist stripper and perform a lift-off of the MoO_x/In/SiO_2 film stack. Rinse the sample using isopropyl alcohol and dry it by blowing N_2. **Figure 1b** is a schematic representation of the sample after this step.

1.5.2. Heat up the sample in vacuum (~7 mTorr) in a single-zone hot-wall tube furnace around 560 °C.

1.5.3. Introduce a mixture gas of 10 sccm of phosphine (99.9995%) and 5 sccm of hydrogen (99.999%) into the growth chamber and set up the chamber pressure around 100 Torr by controlling the exhaust valve.

1.5.4. Maintain the growth temperature and let the InP precipitate out of the liquid In until the entire In template is transformed to InP (typically, 15 min is sufficient). Then, cool down the system to room temperature. **Figure 1c** is a schematic image of the sample after this step.

1.6. Source-drain electrodes pattern lithography and metal evaporation

1.6.1. Repeat steps 1.2.1 through 1.2.4 using a photolithography mask relevant to patterning source-drain electrodes aligned to the InP stripes of the template in step 1.5.4.

1.6.2. Attach the patterned sample from step 1.6.1 to the stage of an e-beam evaporator by polyimide tape. Load Ge, Au, and Ni metal sources in graphite crucibles and pump down the evaporator to a base pressure of ~1 x 10^{-6} Torr.

1.6.3. Engage the high-voltage and gun control of e-beam evaporator, and consecutively evaporate 6 nm of Ge, 10 nm of Au, 80 nm of Ni, and 10 nm of Au.

1.6.4. Immerse the sample in a suitable resist stripper for about 15 min to perform a lift-off to obtain source-drain electrodes. Rinse the sample using isopropyl alcohol and dry it under N_2.

1.6.5. Perform a rapid thermal annealing of the sample in forming gas (5% H_2 and 95% N_2) at an ambient temperature of 380 °C for 15 min.

1.7. Gate dielectric oxide layer deposition

1.7.1. Deposit 60 nm of Al_2O_3 on the entire sample from step 1.6.5 by atomic layer deposition (ALD) at 200 °C, using 97% trimethylaluminum (TMA) and molecular biology grade water (H_2O) as precursors.

1.8. Gate electrode lithography and gate metal deposition

1.8.1. Repeat steps 1.2.1 through 1.2.4 using a photolithography mask relevant to patterning the gate electrode on the sample from step 1.7.1.

1.8.2. Evaporate by attaching the sample to the stage of an e-beam evaporator using polyimide tape and pumping down to a base pressure of about 1 x 10^{-6} Torr.

1.8.3. Engage the high voltage and gun control of the e-beam evaporator and evaporate 80 nm of Ni at a rate of 4 Å/s.

1.8.4. Immerse the sample in a suitable resist stripper and perform a lift-off to obtain gate electrodes. Rinse the sample with isopropyl alcohol and dry it with N_2.

1.9. Via lithography and oxide layer wet etching

1.9.1. Repeat steps 1.2.1 through 1.2.4 using a photolithography mask relevant to patterning source-drain vias on the sample from step 1.8.4.

1.9.2. Etch Al_2O_3 beneath the vias, by hydrofluoric acid solution (HF 50%). A typical process to remove 60 nm of Al_2O_3 is to use 50% HF:H_2O::1:10 for 30 s. Rinse the sample using deionized water.

CAUTION: Hydrofluoric acid is highly corrosive and should be handled with caution while wearing the necessary personal protective equipment.

1.9.3. Strip the resist film in a suitable resist stripper and dry it by blowing N_2 on it. **Figure 1d** is a schematic image of the sample after this step (the end of the fabrication).

2. Synaptic Performance Characterization

2.1. Pulse amplitude-dependent plasticity

2.1.1. Place the sample in the probe station and connect the probes to the gate, source, and drain contact pads.

2.1.2. Connect the gate probe to a voltage pulse generator and the source and drain contacts to source-measurement units (SMUs) of a semiconductor parameter analyzer. Ground the source and apply a constant voltage of 3 V to the drain.

2.1.3. Define the gate voltage as the presynaptic neuron action potential and the source-drain current as the postsynaptic current.

2.1.4. Apply rectangular pulses of varying amplitude and polarity, from -5 V to 5 V, and of a suitable constant pulse width of anything between 500 µs to 5 ms that would mimic a biological pulse time.

2.1.5. Read the source-drain current for each applied pulse for 20 s before and for 40 s after the application of the pulse.

2.1.6. Calculate the synaptic weight change as follows.

2.1.6.1. Define the short-term plasticity as the difference between the average postsynaptic current (PSC) for 1 s before and after the application of the pulse, normalized to that before the pulse.

$$\Delta w_{STP} = \frac{< PSC >_{\text{0 to 1 s after pulse}} - < PSC >_{\text{0 to 1 s before pulse}}}{< PSC >_{\text{0 to 1 s before pulse}}}$$

2.1.6.2. Define the long-term plasticity as the difference between the normalized average PSC between 10 and 40 s after the pulse, and that before the pulse.

$$\Delta w_{LTP} = \frac{< PSC >_{\text{10 to 40 s after pulse}} - < PSC >_{\text{20 s before pulse}}}{< PSC >_{\text{20 s before pulse}}}$$

2.1.6.3. Define zero plasticity as elasticity, positive plasticity as potentiation, and negative plasticity as depression.

2.1.6.4. Plot the synaptic weight change *versus* the gate voltage to, ideally, get an exponential dependence: $\Delta w = A \times e^{V_{gp}/V_a}$, where V_{gp} is the peak gate voltage, and V_a is the activation voltage for the traps.

2.2. Metaplasticity

2.2.1. Repeat steps 2.1.1. through 2.1.3.

2.2.2. Define the priming pulse as a presynaptic action potential that changes the initial state of the synapse before the arrival of the main presynaptic action potential.

2.2.3. Design three sets of experiments: without priming pulse, with depressing priming pulse (such as 2.5 V), and with potentiating priming pulse (such as -2.5 V).

2.2.4. For each set, apply the presynaptic action potential priming pulse and start measuring the source-drain current.

Note: Skip this step for the experiment without priming pulse.

2.2.5. At 10 s, apply varying gate pulses similar to those described in step 2.1.4. Read the source-drain current for 40 s after the application of the main presynaptic pulse.

2.2.6. Repeat step 2.1.6 for each of the three sets of step 2.2.3.

2.3. Spike number-dependent plasticity

2.3.1. Repeat steps 2.1.1 through 2.1.3.

2.3.2. Apply potentiating pulse trains with pulses of fixed amplitude to the presynaptic gate (such as -5 V), of a varying number between 1 and 100, and of a suitable constant pulse width (such as 5 ms pulse width and 5.5 ms period). Repeat step 2.1.5.

2.3.3. Repeat step 2.3.2 but, this time, with depressing pulse trains with pulses of fixed amplitude (such as 5 V).

2.3.4. Plot the long-term and short-term plasticity *versus* the number of action potentials. The trend should initially be increasing and, then, saturating at a higher number of action potentials.

2.4. Spike-timing-dependent plasticity

2.4.1. Repeat step 2.1.1.

2.4.2. Connect the gate and drain probes to separate channels of a voltage pulse generator and the source contact to an SMU of a semiconductor parameter analyzer. Ground the source contact.

2.4.3. Define the gate voltage as the presynaptic neuron action potential, the drain voltage as the postsynaptic neuron action potential, and the source-drain current as the postsynaptic current.

Note: Presynaptic action potential is a bipolar pulse with a small pulse width, such as 10 ms. Reflected postsynaptic action potential is a time-dilated version of the presynaptic action potential with a larger pulse width, such as 100 ms.

2.4.4. Choose the presynaptic action potential and the baseline postsynaptic action potential so that they result in elasticity upon the application of presynaptic action potential at the baseline postsynaptic action potential condition.

2.4.5. Apply presynaptic action potential. Apply postsynaptic action potential with both time lead and lag.

2.4.6. Plot the long-term synaptic weight change *versus* the time difference.

Note: The trend should be maximum potentiation for minimum positive time correlation and maximum depression for minimum negative time correlation. The synaptic weight change should asymptotically approach elasticity with increasing negative and positive time correlation.

REPRESENTATIVE RESULTS:

Figures 1a - **1d** schematically show the fabrication of an artificial synaptic device array based on InP nanostripe FETs on an Si/SiO_2 substrate as described in the protocol section 1. **Figure 2a** is a schematic of a biological synapse, and the analogous parts in the InP channel FET-based artificial synapse are shown in **Figure 2b**.

The output characteristics of a 2 x 4 array of devices shown in **Figures 3a** - **3h** demonstrate the fair uniformity of device performance across different devices. The average effective mobility extracted from the output and transfer curves of each device is around 200 $cm^2/V{\cdot}s$ at a 3-V gate

voltage overdrive with peak effective mobility around 500 $cm^2/V{\cdot}s$, which is more than 10x higher than most carbon nanotube network devices with a peak mobility of 5 - 20 $cm^2/V{\cdot}s$.

The hysteretic transfer characteristics shown in **Figure 4a** demonstrate a potentiation for a gate voltage traverse of 0 to -5 to 0 V and a depression for a gate voltage traverse of 0 to 5 to 0 V. On the other hand, as shown in **Figure 4b**, a peak voltage of 0.7 V leads to elasticity with no change in the postsynaptic current (although a peak voltage of -0.7 V still leads to potentiation). A temporal variation of a postsynaptic current showing typical potentiation, depression, and elasticity is shown in **Figure 4c**. Also based on the definition of short-term plasticity and long-term plasticity in the protocol, the synaptic weight change *versus* presynaptic spike amplitude and polarity has been plotted, as shown in **Figure 4d**, and has been fitted with an exponential curve.

To emulate metaplasticity, representative results from a gate voltage pulse train consisting of 10 pulses of ± 4.5 V of 5-ms width and a 6-ms period as the main depressing/potentiating signals are shown in this work. The artificial synapses were either left unprimed or primed with ± 2.5-V depression/potentiation pulse trains. As shown in **Figure 5a**, the -4.5-V pulse train at t = 0 gives a higher chance of a postsynaptic current when succeeding a depressing priming than a potentiating priming. Similarly, the 4.5-V pulse train at t = 0 gives a greater depression when preceded by a potentiating priming than when it is preceded by a depressing priming, as shown in **Figure 5b**. The short-term plasticity for a gate voltage ranging between -5 and 5 V for no priming, depressing priming, and potentiating priming is shown in **Figure 5c**. A consistent trend of increased potentiation for an initially depressed synapse while a decreased potentiation for an initially potentiated synapse is seen. The analogous observation holds for the effect of the synapse to the depressing signal under different initial states.

To emulate the spike number-dependent plasticity, postsynaptic currents have also been plotted for a varying number of spikes, as shown in **Figure 6a**. Both an increased potentiation and a depression with an increasing spike number are observed as expected.

An initially increasing and, thereafter, saturating trend is demonstrated by plotting the long-term and short-term synaptic weight change for an increased number of action potentials, as shown in **Figures 6b** - **6c**. The synaptic weight change initially increases with an increasing number of action potentials, but with a higher number of action potentials, the weight change approaches saturation because of the finite number of trap states accessible by the particular pulse amplitude.

Finally, the emulation of STDP, which is one of the forms of Hebbian learning[60], is demonstrated. The pulse waveforms for pre- and reflected postsynaptic action potentials are shown in **Figure 7a**. The long-term synaptic weight change *versus* Δt, where Δt is the relative position between pre- and postsynaptic action potentials, is plotted in **Figure 7b**. It can be observed that the maximum amplitudes of potentiation and depression are achieved at the smallest values of Δt. For longer time intervals, the amplitude of both potentiation and depression decreases and approaches elasticity as expected.

FIGURE AND TABLE LEGENDS:

Figure 1: Schematic of TLP growth. (**a** - **d**) Schematic of the TLP growth of single-crystalline InP nanostripe field-effect transistor arrays on Si/SiO_2 substrate. Reprinted (adapted) with permission from Kim *et al*.[57], copyright 2018 American Chemical Society.

Figure 2: Schematics of a biological synapse and an InP nanostripe FET artificial synapse. (**a**) Schematic of a biological synapse. (**b**) Schematic of an InP nanostripe FET artificial synapse. Reprinted (adapted) with permission from Kim *et al*.[57], copyright 2018 American Chemical Society.

Figure 3: Output characteristics of an array of transistors. (**a** - **d**) These panels show the output characteristics of an array of transistors of 10 µm in length at V_{gs} = 0, 1, 2, 3 V. (**e** - **h**) These panels show the output characteristics of an array of transistor of 25 µm in length at V_{gs} = 0, 1, 2, 3 V. Reprinted (adapted) with permission from Kim *et al*.[57], copyright 2018 American Chemical Society.

Figure 4: Spike amplitude-dependent plasticity. (**a**) This panel shows hysteretic transfer characteristics showing depression for 5 V and potentiation for -5 V. (**b**) This panel shows hysteretic transfer characteristics showing elasticity for 0.7 V and potentiation for -0.7 V. (**c**) This panel shows the transient postsynaptic current before and after the application of single presynaptic pulse, leading to elasticity (0.1 V), potentiation (-5 V), and depression (+5 V). (**d**) This panel shows short-term and long-term synaptic weight change for different values of a presynaptic voltage pulse. All curves are reported with V_{ds} = 3 V. Reprinted (adapted) with permission from Kim *et al*.[57], copyright 2018 American Chemical Society.

Figure 5: Synaptic metaplasticity. (**a**) This panel shows an increased potentiation of synapse succeeding a depressing priming compared to potentiating priming. (**b**) This panel shows an increased depression of synapse succeeding a potentiating priming compared to depressing priming. (**c**) This panel shows short-term synaptic weight change for different values of presynaptic voltage pulse without priming, and with depressing and potentiating priming. Reprinted (adapted) with permission from Kim *et al*.[57], copyright 2018 American Chemical Society.

Figure 6: Spike number-dependent plasticity. (**a**) This panel shows a transient postsynaptic current before and after the application of a presynaptic pulse for varying pulse numbers, nAP = 1, 20, 100. (**b**) This panel shows the variation of a short-term synaptic relaxation time constant with a different number of action potentials. The last two panels show (**c**) a long-term and (**d**) a short-term synaptic weight change for a different number of potentiating and depressing action potentials. Reprinted (adapted) with permission from Kim *et al*.[57], copyright 2018 American Chemical Society.

Figure 7: Spike-timing-dependent plasticity. (**a**) This panel shows waveforms representing a back-reflected postsynaptic action potential (upper row) and presynaptic action potential (lower row) for a presynaptic action potential preceding (left column) and succeeding (right column) the reflected postsynaptic action potential. (**b**) This panel shows the long-term synaptic weight

change for different values of time, offset between the pre- and postsynaptic action potentials. Reprinted (adapted) with permission from Kim *et al*.[57], copyright 2018 American Chemical Society.

DISCUSSION:

Several steps in the protocol deserve discussion. First, in the growth of InP nanostripes, the P flux needs to be tuned as described in previous works[62], to ensure single nucleation in individual channels from which the entire channel grows out, resulting in the single crystallinity of the grown materials. A polycrystalline InP stripe would reduce mobility, thus reducing transconductance, which means the synaptic weight change, which is directly proportional to the transconductance, would also be reduced.

Second, to ensure the wetting of the In templates, the geometry of the template has to be critically maintained. Working within the realms allowed by standard photolithography, a channel width of 2 µm would require 200-nm or thicker In to wet the SiO_2 surface with a SiO_2 capping layer[66]. However, at that thickness, it would be difficult to deplete the entire channel by the gate voltage. Therefore, a thin layer of ~5 nm of MoO_x is deposited, which tunes the surface energies favorably to allow the wetting of 100-nm-thick In.

Third, while an InP-based FET has been demonstrated here as a proof of concept, a multitude of compound semiconductor materials that conform to the TLP growth methodology, such as high-mobility InGaAs, high-bandgap GaN, *etc.*, can potentially be used and chosen according to the application requirements.

Fourth, an important device characteristic is stability over time. Unlike several other material and device classes that have been used to show synaptic behavior, the InP FETs discussed here have been found to be stable over several years despite being stored in normal ambient conditions.

Fifth, an important aspect of the neuromorphic computing paradigm includes hardware implementation with a reduced footprint[1]. It may be noted that this protocol for artificial synaptic devices harnesses the different unique advantages of TLP growth, including scalability and growth in deterministic position and geometry, to obtain single-device synaptic implementation. Although the devices shown here are in the micron scale for proof-of-concept demonstration, it can be easily realized that, with existing fabrication capabilities, the footprint is significantly reduced to the nanometer scale in the future.

Sixth, arguably the most important aspect of neuromorphic computing is energy efficiency in handling large datasets. This can be achieved by an optimal choice of the pulse width and amplitude. It may be noted that, here, hundreds of microseconds to a few millisecond scale pulse widths are chosen, which conforms to biological neuronal spiking standards. The pulse amplitudes are relatively higher than usual, stemming from the relatively thick gate oxide used here. However, this can also be taken care of, by suitably designing a scaled device.

ACKNOWLEDGMENTS:

R.K. acknowledges funding from the National Science Foundation (award no. 1610604). J.T. thanks the support by the USC Provost Graduate Fellowship. D.S. thanks the support by the USC Annenberg Graduate Fellowship. The authors gratefully acknowledge the use of the ALD facility and PL system in Stephen Cronin's Lab.

DISCLOSURES:

The authors have nothing to disclose.

REFERENCES:

1. Schuller, I. K., Stevens, R. Neuromorphic computing: from materials to systems architecture. *Report of a Roundtable Convened to Consider Neuromorphic Computing Basic Research Needs* (2015).

2. Mead, C. Neuromorphic electronic systems. *Proceedings of the IEEE.* **78** (10), 1629-1636 (1990).

3. Mead, C., Ismail, M. *Analog VLSI Implementation of Neural Systems*. Springer Science & Business Media (2012).

4. Merolla, P. A. *et al.* A million spiking-neuron integrated circuit with a scalable communication network and interface. *Science.* **345** (6197), 668-673 (2014).

5. Hsu, J. Ibm's new brain [news]. *IEEE Spectrum.* **51** (10), 17-19 (2014).

6. Furber, S. B., Galluppi, F., Temple, S., Plana, L. A. The spinnaker project. *Proceedings of the IEEE.* **102** (5), 652-665 (2014).

7. Farquhar, E., Hasler, P. A bio-physically inspired silicon neuron. *IEEE Transactions on Circuits and Systems I: Regular Papers.* **52** (3), 477-488 (2005).

8. Rangan, V., Ghosh, A., Aparin, V., Cauwenberghs, G. A subtrheshold aVLSI implementation of the Izhikevich simple neuron model. *Proceedings of the 2010 Annual Internation Conference of the IEEE Engineering in Medicine and Biology Society*. **2010**, 4164-4167 (2010).

9. Indiveri, G. *et al.* Neuromorphic silicon neuron circuits. *Frontiers in Neuroscience.* **5** (2011).

10. Chicca, E., Indiveri, G., Douglas, R. An adaptive silicon synapse. *Proceedings of the 2003 International Symposium on Circuits and Systems (ISCAS)* (2003)

11. Bartolozzi, C., Indiveri, G. Synaptic dynamics in analog VLSI. *Neural Computation.* **19** (10), 2581-2603 (2007).

12. Friesz, A. K. *et al.* "A biomimetic carbon nanotube synapse circuit." *Biomedical Engineering Society (BMES) Annual Fall Meeting*. **2** (8) (2007).

13. Arthur, J. V., Kwabena B. "Learning in silicon: Timing is everything." *Advances in Neural Information Processing Systems 18*. 75-82 (December 5 - 8, 2005).

14. Azghadi, M. R., Iannella, N., Al-Sarawi, S. F., Indiveri, G., Abbott, D. Spike-based synaptic plasticity in silicon: design, implementation, application, and challenges. *Proceedings of the IEEE.* **102** (5), 717-737 (2014).

15. Benjamin, B. V. *et al.* Neurogrid: A mixed-analog-digital multichip system for large-scale neural simulations. *Proceedings of the IEEE.* **102** (5), 699-716 (2014).

16. Furber, S. Large-scale neuromorphic computing systems. *Journal of Neural Engineering.* **13** (5), 051001 (2016).

17. Purves, D. E., Augustine, G. J., Fitzpatrick, D. E., Katz, L. C. *Neuroscience*. Sinauer Associates (1997).

18. Striedter, G. F. *Neurobiology: A Functional Approach*. Oxford University Press (2015).

19. Tan, Z. H. *et al.* Synaptic metaplasticity realized in oxide memristive devices. *Advanced Materials.* **28** (2), 377-384 (2016).

20. Zhu, X., Du, C., Jeong, Y., Lu, W. D. Emulation of synaptic metaplasticity in memristors. *Nanoscale.* **9** (1), 45-51 (2017).

21. Arnold, A. J. *et al.* Mimicking Neurotransmitter Release in Chemical Synapses via Hysteresis Engineering in MoS2 Transistors. *ACS Nano.* **11** (3), 3110-3118 (2017).

22. Hebb, D. O. *The Organization of Behavior: A Neuropsychological Approach*. John Wiley & Sons (1949).

23. Bienenstock, E. L., Cooper, L. N., Munro, P. W. Theory for the development of neuron selectivity: orientation specificity and binocular interaction in visual cortex. *Journal of Neuroscience.* **2** (1), 32-48 (1982).

24. Markram, H., Lübke, J., Frotscher, M., Sakmann, B. Regulation of synaptic efficacy by coincidence of postsynaptic APs and EPSPs. *Science.* **275** (5297), 213-215 (1997).

25. Bi, G.-q., Poo, M.-m. Synaptic modifications in cultured hippocampal neurons: dependence on spike timing, synaptic strength, and postsynaptic cell type. *Journal of Neuroscience.* **18** (24), 10464-10472 (1998).

26. Van Rossum, M. C. W., Bi, G. Q., Turrigiano, G. G. Stable Hebbian learning from spike timing-dependent plasticity. *Journal of Neuroscience.* **20** (23), 8812-8821 (2000).

27. Pickett, M. D., Medeiros-Ribeiro, G., Williams, R. S. A scalable neuristor built with Mott memristors. *Nature Materials.* **12** (2), 114-117 (2013).

28. Krzysteczko, P., Münchenberger, J., Schäfers, M., Reiss, G., Thomas, A. The Memristive Magnetic Tunnel Junction as a Nanoscopic Synapse-Neuron System. *Advanced Materials.* **24** (6), 762-766 (2012).

29. Jeong, D. S., Kim, I., Ziegler, M., Kohlstedt, H. Towards artificial neurons and synapses: a materials point of view. *RSC Advances.* **3** (10), 3169-3183 (2013).

30. Suri, M. *Advances in Neuromorphic Hardware Exploiting Emerging Nanoscale Devices*. Springer (2017).

31. Diorio, C., Hasler, P., Minch, A., Mead, C. A. A single-transistor silicon synapse. *IEEE Transactions on Electron Devices.* **43** (11), 1972-1980 (1996).

32. Lai, Q. *et al.* Ionic/electronic hybrid materials integrated in a synaptic transistor with signal processing and learning functions. *Advanced Materials.* **22** (22), 2448-2453 (2010).

33. Alibart, F. *et al.* An organic nanoparticle transistor behaving as a biological spiking synapse. *Advanced Functional Materials.* **20** (2), 330-337 (2010).

34. Tian, H. *et al.* Anisotropic black phosphorus synaptic device for neuromorphic applications. *Advanced Materials.* **28** (25), 4991-4997 (2016).

35. Xu, W., Min, S.-Y., Hwang, H., Lee, T.-W. Organic core-sheath nanowire artificial synapses with femtojoule energy consumption. *Science Advances.* **2** (6), e1501326 (2016).

36. Strukov, D. B., Snider, G. S., Stewart, D. R., Williams, R. S. The missing memristor found. *Nature.* **453** (7191), 80 (2008).

37. Kuzum, D., Jeyasingh, R. G. D., Lee, B., Wong, H. S. P. Nanoelectronic programmable synapses based on phase change materials for brain-inspired computing. *Nano Letters.* **12** (5), 2179-2186 (2011).

38. Chanthbouala, A. *et al.* A ferroelectric memristor. *Nature Materials.* **11** (10), 860-864 (2012).

39. Zuo, F. *et al.* Habituation based synaptic plasticity and organismic learning in a quantum perovskite. *Nature Communications.* **8** (1), 240 (2017).

40. Chang, T., Jo, S.-H., Lu, W. Short-term memory to long-term memory transition in a nanoscale memristor. *ACS Nano.* **5** (9), 7669-7676 (2011).

41. Ohno, T. *et al.* Short-term plasticity and long-term potentiation mimicked in single inorganic synapses. *Nature Materials.* **10** (8), 591-595 (2011).

42. Wang, Z. Q. *et al.* Synaptic learning and memory functions achieved using oxygen ion migration/diffusion in an amorphous InGaZnO memristor. *Advanced Functional Materials.* **22** (13), 2759-2765 (2012).

43. Mayr, C. *et al.* "Waveform driven plasticity in BiFeO3 memristive devices: model and implementation." *Advances in Neural Information Processing Systems*, 1700-1708 (December 3 - 6, 2012)

44. Subramaniam, A., Cantley, K. D., Bersuker, G., Gilmer, D. C., Vogel, E. M. Spike-timing-dependent plasticity using biologically realistic action potentials and low-temperature materials. *IEEE Transactions on Nanotechnology.* **12** (3), 450-459 (2013).

45. Williamson, A. *et al.* Synaptic behavior and STDP of asymmetric nanoscale memristors in biohybrid systems. *Nanoscale.* **5** (16), 7297-7303 (2013).

46. Ambrogio, S., Balatti, S., Nardi, F., Facchinetti, S., Ielmini, D. Spike-timing dependent plasticity in a transistor-selected resistive switching memory. *Nanotechnology.* **24** (38), 384012 (2013).

47. Shi, J., Ha, S. D., Zhou, Y., Schoofs, F., Ramanathan, S. A correlated nickelate synaptic transistor. *Nature Communications.* **4**, 2676 (2013).

48. Du, C., Ma, W., Chang, T., Sheridan, P., Lu, W. D. Biorealistic implementation of synaptic functions with oxide memristors through internal ionic dynamics. *Advanced Functional Materials.* **25** (27), 4290-4299 (2015).

49. Kim, S. *et al.* Experimental demonstration of a second-order memristor and its ability to biorealistically implement synaptic plasticity. *Nano Letters.* **15** (3), 2203-2211 (2015).

50. Wang, Z. *et al.* Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing. *Nature Materials.* **16** (1), 101-108 (2017).

51. La Barbera, S., Vuillaume, D., Alibart, F. Filamentary switching: synaptic plasticity through device volatility. *ACS Nano.* **9** (1), 941-949 (2015).

52. Lai, Q. *et al.* Analog memory capacitor based on field-configurable ion-doped polymers. *Applied Physics Letters.* **95** (21), 213503 (2009).

53. Najem, J. S. *et al.* Memristive Ion Channel-Doped Biomembranes as Synaptic Mimics. *ACS Nano.* **12** (5), 4702-4711 (2018).

54. Li, C. *et al.* Analogue signal and image processing with large memristor crossbars. *Nature Electronics.* **1** (1), 52 (2018).

55. Wu, C., Kim, T. W., Choi, H. Y., Strukov, D. B., Yang, J. J. Flexible three-dimensional artificial synapse networks with correlated learning and trainable memory capability. *Nature Communications.* **8** (1), 752 (2017).

56. Kim, S., Yoon, J., Kim, H.-D., Choi, S.-J. Carbon nanotube synaptic transistor network for pattern recognition. *ACS Applied Materials & Interfaces.* **7** (45), 25479-25486 (2015).

57. Kim, S. *et al.* Pattern Recognition Using Carbon Nanotube Synaptic Transistors with an Adjustable Weight Update Protocol. *ACS Nano.* **11** (3), 2814-2822 (2017).

58. Shen, A. M. *et al.* Analog neuromorphic module based on carbon nanotube synapses. *ACS Nano.* **7** (7), 6117-6122 (2013).

59. Kim, K., Chen, C. L., Truong, Q., Shen, A. M., Chen, Y. A carbon nanotube synapse with dynamic logic and learning. *Advanced Materials.* **25** (12), 1693-1698 (2013).

60. Kapadia, R. *et al.* A direct thin-film path towards low-cost large-area III-V photovoltaics. *Scientific Reports.* **3**, srep02275 (2013).

61. Kapadia, R. *et al.* Deterministic nucleation of InP on metal foils with the thin-film vapor–liquid–solid growth mode. *Chemistry of Materials.* **26** (3), 1340-1344 (2014).

62. Chen, K. *et al.* Direct growth of single-crystalline III–V semiconductors on amorphous substrates. *Nature Communications.* **7**, 10502 (2016).

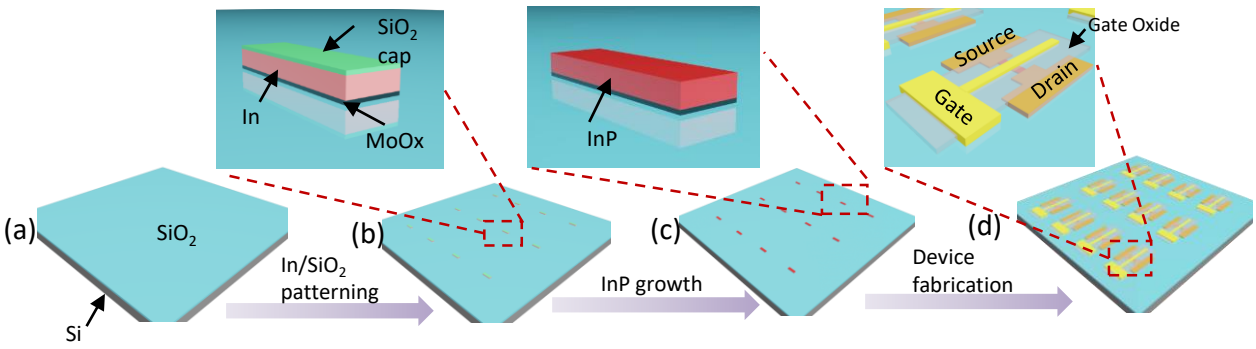
63. Lin, Q. *et al.* Scalable Indium Phosphide Thin-Film Nanophotonics Platform for Photovoltaic and Photoelectrochemical Devices. *ACS Nano.* **11** (5), 5113-5119 (2017).

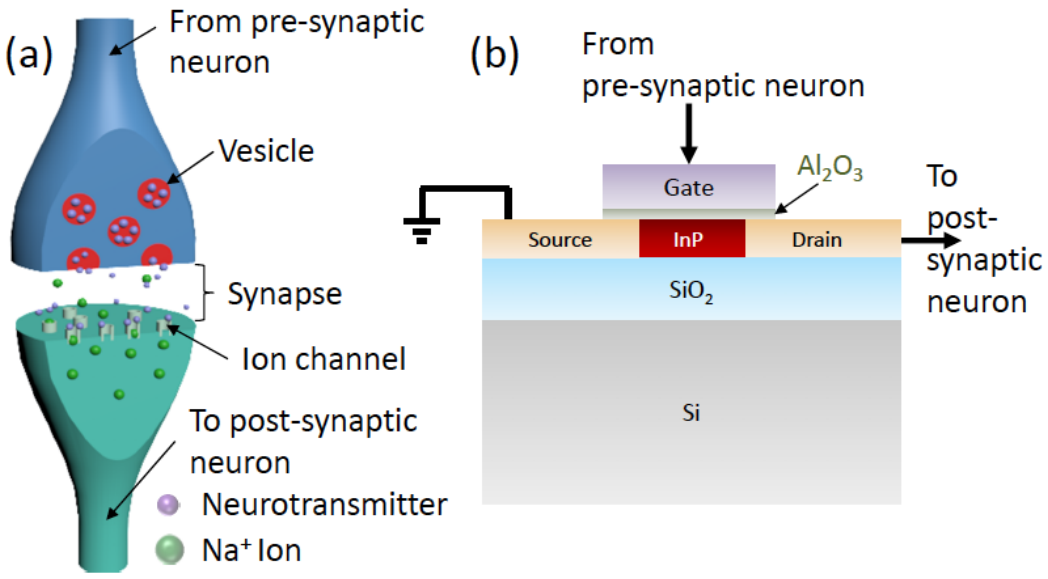
64. Sarkar, D. *et al.* Mimicking Biological Synaptic Functionality with an Indium Phosphide Synaptic Device on Silicon for Scalable Neuromorphic Computing. *ACS Nano.* **12** (2), 1656-1663 (2018).

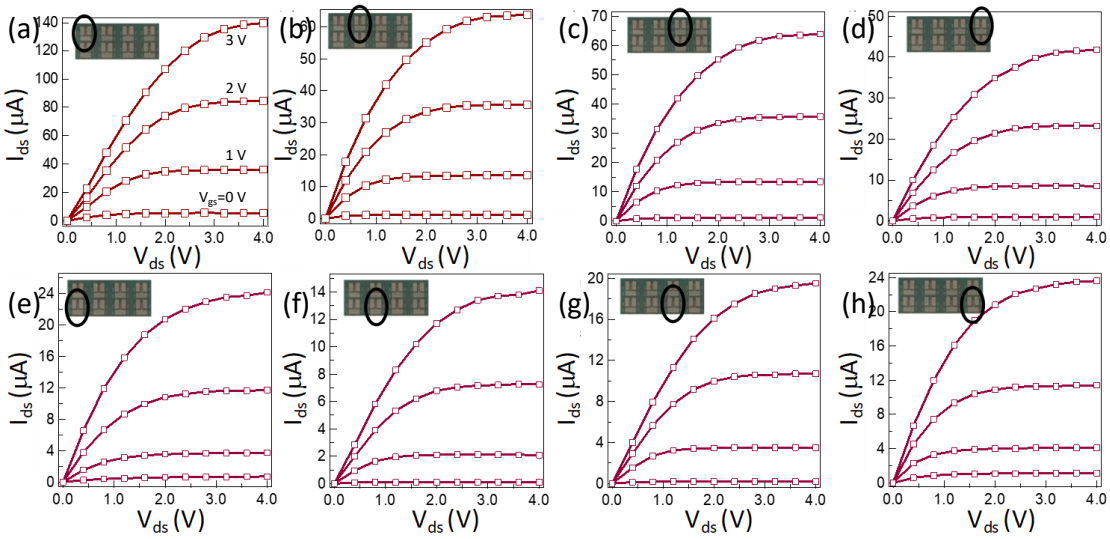
65. Sarkar, D. *et al.* Buffer insensitive optoelectronic quality of InP-on-Si with templated liquid phase growth. *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena.* **36** (3), 031204 (2018).

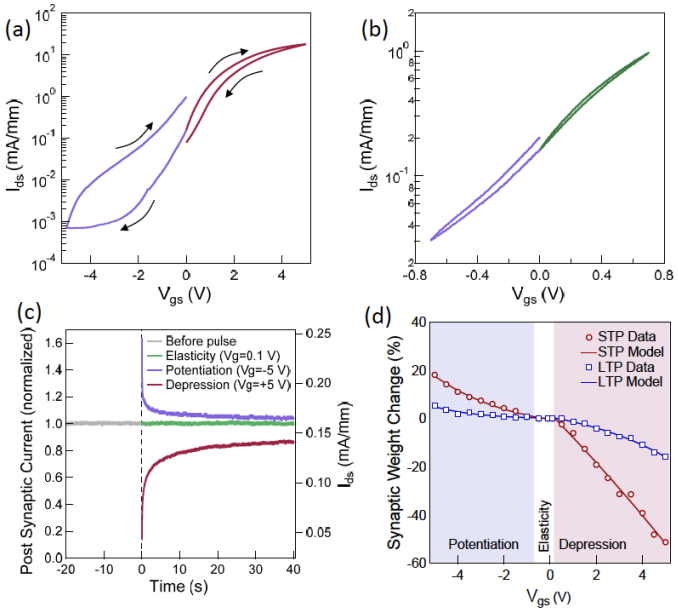
66. Sarkar, D. *et al.* Confined Liquid Phase Growth of Crystalline Compound Semiconductors on Any Substrate. *ACS Nano.* **12** (6), 5158-5167 (2018).

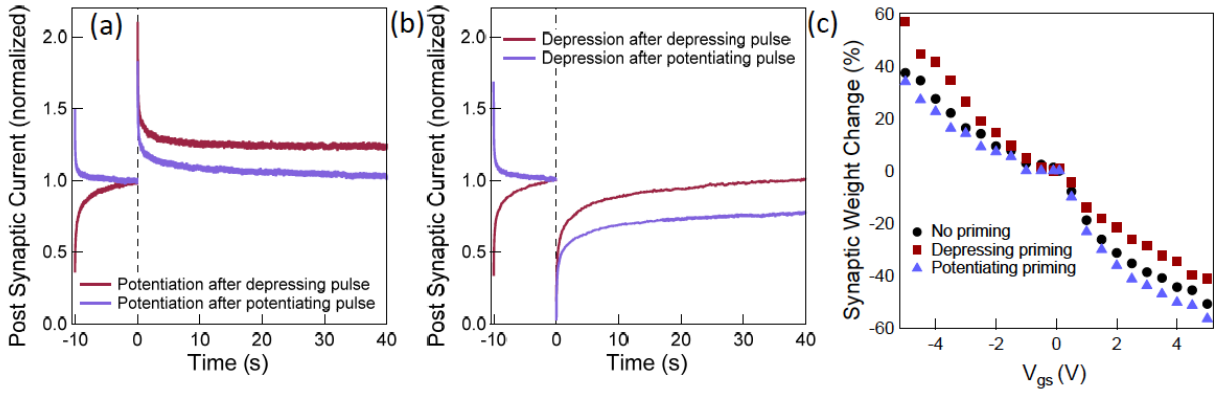
Figure 1

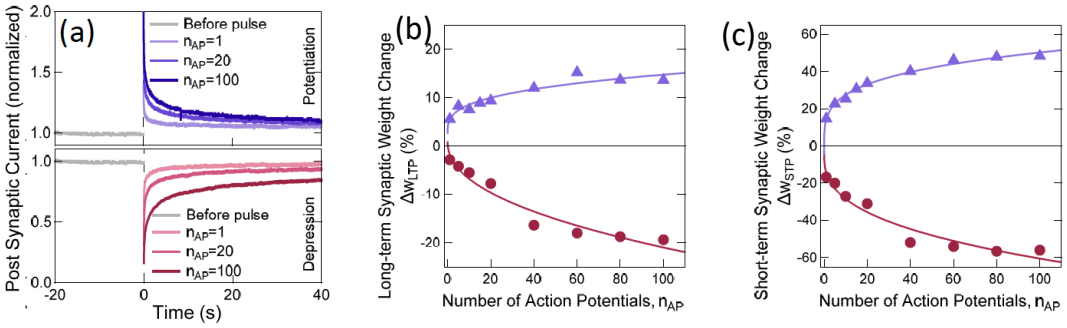



(a)
From pre-synaptic neuron
Vesicle
Synapse
Ion channel
To post-synaptic neuron
Neurotransmitter
Na+ Ion
(b)
From pre-synaptic neuron
Gate
Al2O3
Source
InP
Drain
To post-synaptic neuron
SiO2
Si


(a)
(b)
(c)
(d)
(e)
(f)
(g)
(h)
3 V
2 V
1 V
V_{gs}=0 V
I_{ds} (μA)
V_{ds} (V)


(a)
I_{ds} (mA/mm)
V_{gs} (V)
(b)
I_{ds} (mA/mm)
V_{gs} (V)
(c)
Before pulse
Elasticity (Vg=0.1 V)
Potentiation (Vg=-5 V)
Depression (Vg=+5 V)
Post Synaptic Current (normalized)
I_{ds} (mA/mm)
Time (s)
(d)
STP Data
STP Model
LTP Data
LTP Model
Synaptic Weight Change (%)
Potentiation
Elasticity
Depression
V_{gs} (V)


(a)
Post Synaptic Current (normalized)
Time (s)
Potentiation after depressing pulse
Potentiation after potentiating pulse
(b)
Depression after depressing pulse
Depression after potentiating pulse
(c)
Synaptic Weight Change (%)
No priming
Depressing priming
Potentiating priming
V_{gs} (V)


(a)
Before pulse
n_{AP}=1
n_{AP}=20
n_{AP}=100
Potentiation
Before pulse
n_{AP}=1
n_{AP}=20
n_{AP}=100
Depression
Post Synaptic Current (normalized)
Time (s)
(b)
Long-term Synaptic Weight Change
Δw_{LTP} (%)
Number of Action Potentials, n_{AP}
(c)
Short-term Synaptic Weight Change
Δw_{STP} (%)
Number of Action Potentials, n_{AP}

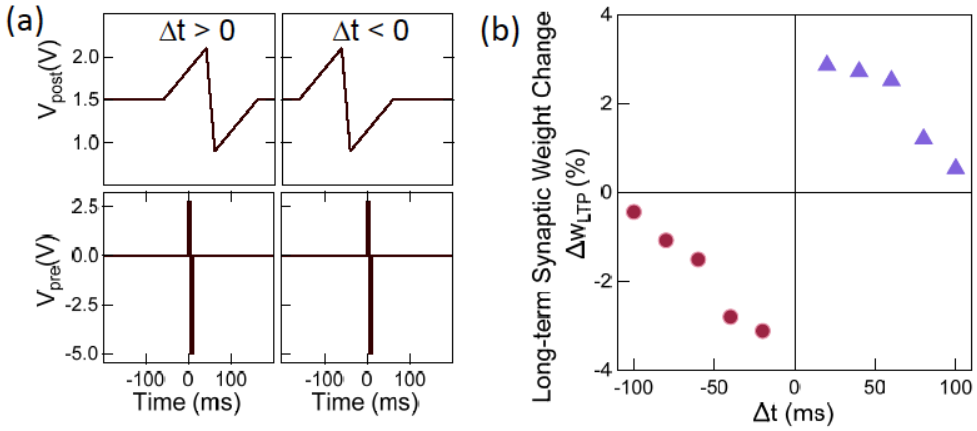

(a)
Δt > 0
Δt < 0
V_post(V)
2.0
1.5
1.0
V_pre(V)
2.5
0.0
-2.5
-5.0
-100
0
100
Time (ms)
(b)
Long-term Synaptic Weight Change
Δw_LTP (%)
4
2
0
-2
-4
-100
-50
0
50
100
Δt (ms)

Figure 2

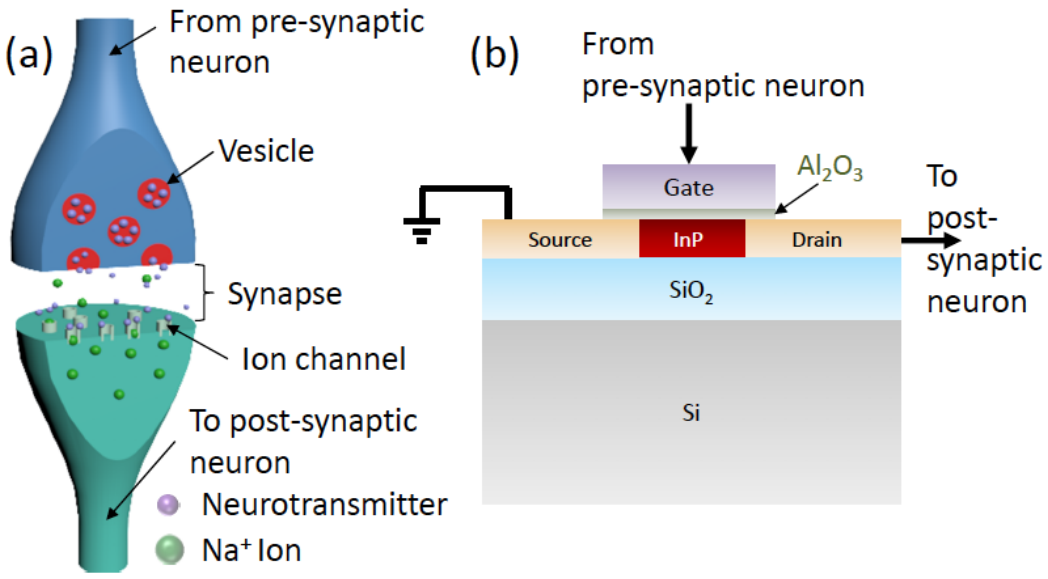


Figure 3

Click here to access/download;Figure;Figure 3 Final.pdf

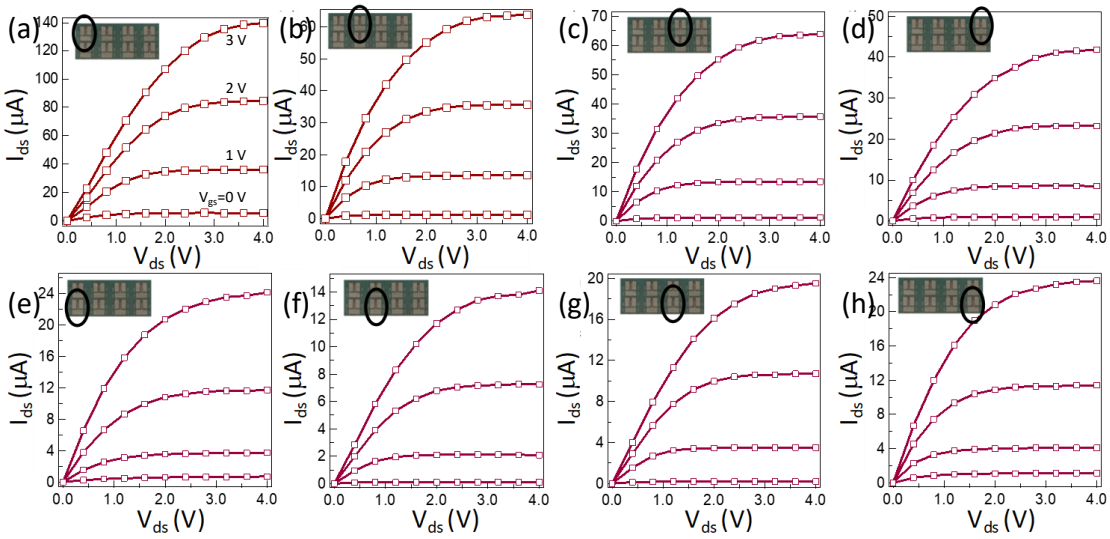


Figure 4

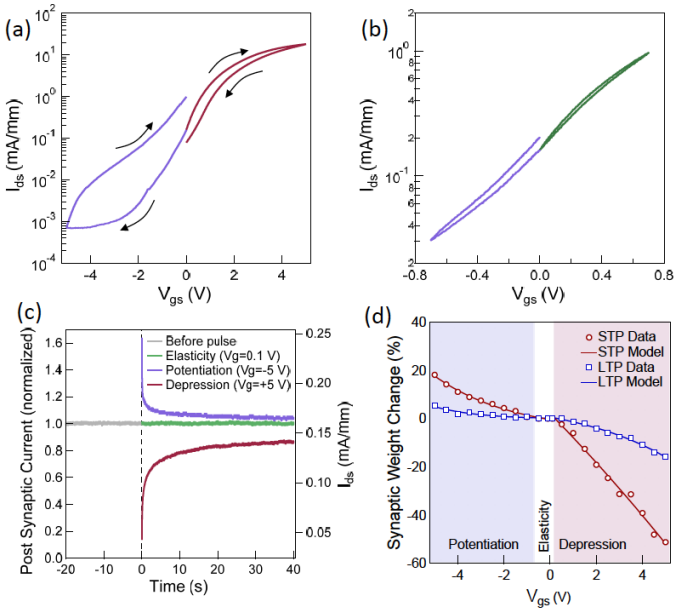


Figure 5

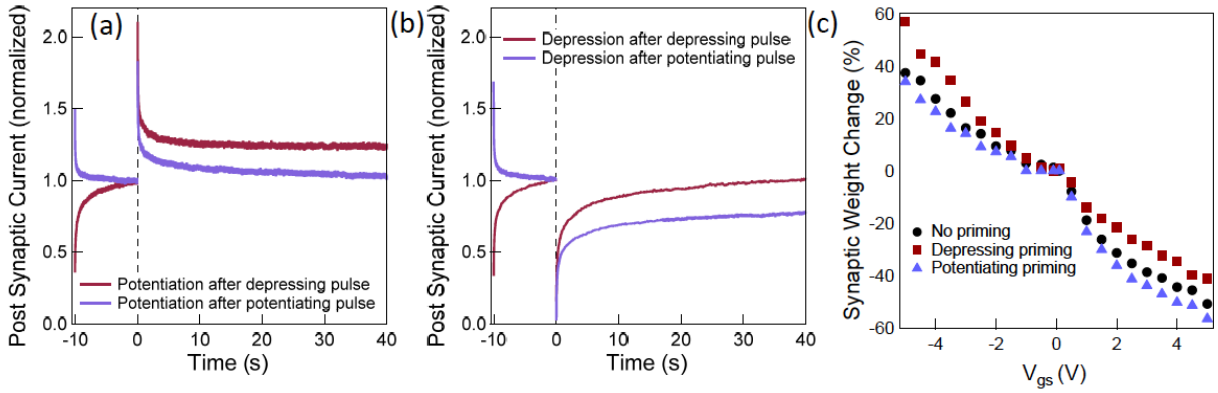


Figure 6

Click here to access/download;Figure;Figure 6 Final.pdf

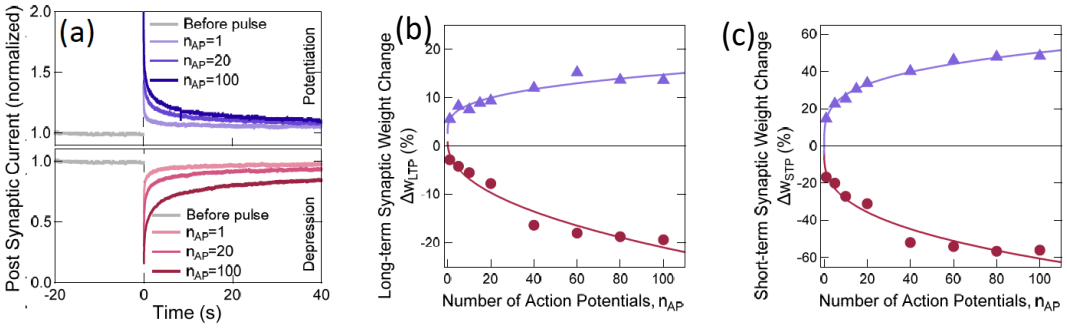
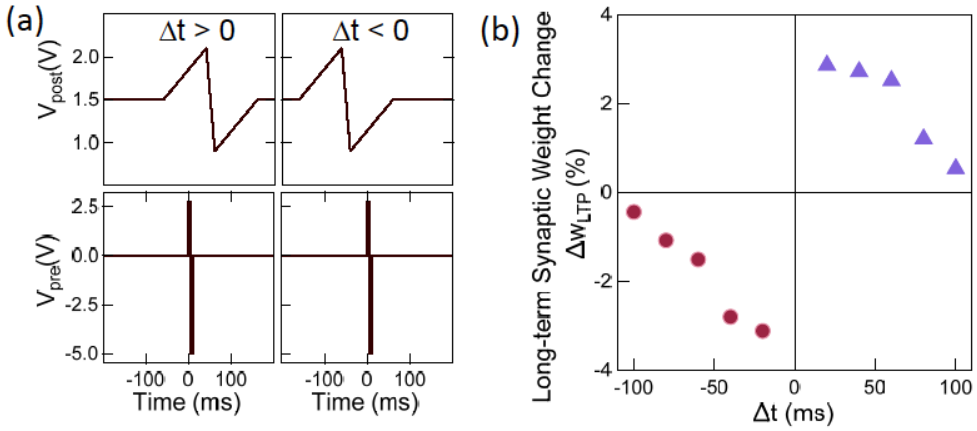


Figure 7



Name of Material/ Equipment	Company	Catalog Number	Comments/Description
Acetone	JT Baker	9005-05	CMOS grade
IPA	JT Baker	9079-05	CMOS grade
DI water	ELGA	Purelabflex 3	
Dry nitrogen	Praxair	N/A	
Oxygen plasma asher	Tegal Co	100-5114	
		G516608	
LOR5A	Microchem	0500L1GL	
AZ5214E IR	Integrated Micro Materials	AZ5214EIR-Q	
Aligner	Karl Suss	100UV030	110V 60Hz
Quartz mask	Photosciences	N/A	Custom designed
MF-319	Dow	DEM-10018042	
Molybdenum (VI) oxide	Alfa Aesar	12930-14	99.9995% pure
Liquid nitrogen	Praxair	N/A	
Alumina coated molyndenum boat	Kurt J Lesker Company	EVSME3AOMO	7/8'' x 3/4'' x 1/8'' deep
Thermal evaporator	Denton Vacuum Inc	DV-502A	
Thermal evaporator	Torr International Inc	THE4-1X2KW-LL	
Indium	Indium Co	SHOT16-47562	99.99995% pure
Electron beam evaporator	Sloan	SL1800	
Electron beam evaporator	Temescal	BJD-1800	
Silicon dioxide	Kurt J Lesker Company	EVMSIO21-5D	99.99% pure
Carbon crucible	Kurt J Lesker Company	EVCFABEB-23	1.125'' TOD x 0.520'' HIGH
PG Remover	Microchem	G0502004000l1PE	
Single-zone hot-wall tube furnace	Thermo Scientific	TF55035A-1	

Phosphine	Matheson	N/A	99.9995% pure
Hydrogen	HOGEN	N/A	99.999% pure
Germanium	Kurt J Lesker Company	EVMGE50500GM	99.999% pure
Gold	Kurt J Lesker Company	EVMAUXX50G	99.999% pure
Nickel	International Advanced Materials	180166	99.999% pure
Rapid thermal annealer	AG Associate	Mini Pulse 310	
Forming gas	Airgas	N/A	98% N2, 2% H2
Atomic layer deposition	Ultratech/Cambridge Savannah ALD	Savannah S100	
Trimethyl aluminum	ALDRICH	1001278062	
Water	ALDRICH	W 4502	
Probe Station	Karl Suss	11500018	
Voltage Pulse Generator	Tektronix	AWG2021	
Semiconductor Parameter Analyzer	Keysight	B1500a	

jove JOURNAL OF VISUALIZED EXPERIMENTS
1 Alewife Center #200
Cambridge, MA 02140
tel. 617.945.9051
www.jove.com

ARTICLE AND VIDEO LICENSE AGREEMENT

Title of Article: Indium phosphide Synaptic Device on Silicon to Emulate Synaptic Behavior for Neuromorphic Computing

Author(s): Debarghya Sarkar, Jun Tao, Wei Wang, Qingfeng Lin, Matthew Yeung, Chenhao Ren, and Rehan Kapadia

Item 1 (check one box): The Author elects to have the Materials be made available (as described at http://www.jove.com/author) via: ☑ Standard Access ☐ Open Access

Item 2 (check one box):

☑ The Author is NOT a United States government employee.

☐ The Author is a United States government employee and the Materials were prepared in the course of his or her duties as a United States government employee.

☐ The Author is a United States government employee but the Materials were NOT prepared in the course of his or her duties as a United States government employee.

ARTICLE AND VIDEO LICENSE AGREEMENT

1. Defined Terms. As used in this Article and Video License Agreement, the following terms shall have the following meanings: "**Agreement**" means this Article and Video License Agreement; "**Article**" means the article specified on the last page of this Agreement, including any associated materials such as texts, figures, tables, artwork, abstracts, or summaries contained therein; "**Author**" means the author who is a signatory to this Agreement; "**Collective Work**" means a work, such as a periodical issue, anthology or encyclopedia, in which the Materials in their entirety in unmodified form, along with a number of other contributions, constituting separate and independent works in themselves, are assembled into a collective whole; "**CRC License**" means the Creative Commons Attribution-Non Commercial-No Derivs 3.0 Unported Agreement, the terms and conditions of which can be found at: http://creativecommons.org/licenses/by-nc-nd/3.0/legalcode; "**Derivative Work**" means a work based upon the Materials or upon the Materials and other pre-existing works, such as a translation, musical arrangement, dramatization, fictionalization, motion picture version, sound recording, art reproduction, abridgment, condensation, or any other form in which the Materials may be recast, transformed, or adapted; "**Institution**" means the institution, listed on the last page of this Agreement, by which the Author was employed at the time of the creation of the Materials; "**JoVE**" means MyJove Corporation, a Massachusetts corporation and the publisher of *The Journal of Visualized Experiments;* "**Materials**" means the Article and / or the Video; "**Parties**" means the Author and JoVE; "**Video**" means any video(s) made by the Author, alone or in conjunction with any other parties, or by JoVE or its affiliates or agents, individually or in collaboration with the Author or any other parties, incorporating all or any portion of the Article, and in which the Author may or may not appear.

2. Background. The Author, who is the author of the Article, in order to ensure the dissemination and protection of the Article, desires to have the JoVE publish the Article and create and transmit videos based on the Article. In furtherance of such goals, the Parties desire to memorialize in this Agreement the respective rights of each Party in and to the Article and the Video.

3. Grant of Rights in Article. In consideration of JoVE agreeing to publish the Article, the Author hereby grants to JoVE, subject to **Sections 4** and **7** below, the exclusive, royalty-free, perpetual (for the full term of copyright in the Article, including any extensions thereto) license (a) to publish, reproduce, distribute, display and store the Article in all forms, formats and media whether now known or hereafter developed (including without limitation in print, digital and electronic form) throughout the world, (b) to translate the Article into other languages, create adaptations, summaries or extracts of the Article or other Derivative Works (including, without limitation, the Video) or Collective Works based on all or any portion of the Article and exercise all of the rights set forth in (a) above in such translations, adaptations, summaries, extracts, Derivative Works or Collective Works and (c) to license others to do any or all of the above. The foregoing rights may be exercised in all media and formats, whether now known or hereafter devised, and include the right to make such modifications as are technically necessary to exercise the rights in other media and formats. If the "Open Access" box has been checked in **Item 1** above, JoVE and the Author hereby grant to the public all such rights in the Article as provided in, but subject to all limitations and requirements set forth in, the CRC License.

4. Retention of Rights in Article. Notwithstanding the exclusive license granted to JoVE in **Section 3** above, the Author shall, with respect to the Article, retain the non-exclusive right to use all or part of the Article for the non-commercial purpose of giving lectures, presentations or teaching classes, and to post a copy of the Article on the Institution's website or the Author's personal website, in each case provided that a link to the Article on the JoVE website is provided and notice of JoVE's copyright in the Article is included. All non-copyright intellectual property rights in and to the Article, such as patent rights, shall remain with the Author.

5. Grant of Rights in Video – Standard Access. This **Section 5** applies if the "Standard Access" box has been checked in **Item 1** above or if no box has been checked in **Item 1** above. In consideration of JoVE agreeing to produce, display or otherwise assist with the Video, the Author hereby acknowledges and agrees that, Subject to **Section 7** below, JoVE is and shall be the sole and exclusive owner of all rights of any nature, including, without limitation, all copyrights, in and to the Video. To the extent that, by law, the Author is deemed, now or at any time in the future, to have any rights of any nature in or to the Video, the Author hereby disclaims all such rights and transfers all such rights to JoVE.

6. Grant of Rights in Video – Open Access. This **Section 6** applies only if the "Open Access" box has been checked in **Item 1** above. In consideration of JoVE agreeing to produce, display or otherwise assist with the Video, the Author hereby grants to JoVE, subject to **Section 7** below, the exclusive, royalty-free, perpetual (for the full term of copyright in the Article, including any extensions thereto) license (a) to publish, reproduce, distribute, display and store the Video in all forms, formats and media whether now known or hereafter developed (including without limitation in print, digital and electronic form) throughout the world, (b) to translate the Video into other languages, create adaptations, summaries or extracts of the Video or other Derivative Works or Collective Works based on all or any portion of the Video and exercise all of the rights set forth in (a) above in such translations, adaptations, summaries, extracts, Derivative Works or Collective Works and (c) to license others to do any or all of the above. The foregoing rights may be exercised in all media and formats, whether now known or hereafter devised, and include the right to make such modifications as are technically necessary to exercise the rights in other media and formats. For any Video to which this Section 6 is applicable, JoVE and the Author hereby grant to the public all such rights in the Video as provided in, but subject to all limitations and requirements set forth in, the CRC License.

7. Government Employees. If the Author is a United States government employee and the Article was prepared in the course of his or her duties as a United States government employee, as indicated in **Item 2** above, and any of the licenses or grants granted by the Author hereunder exceed the scope of the 17 U.S.C. 403, then the rights granted hereunder shall be limited to the maximum rights permitted under such statute. In such case, all provisions contained herein that are not in conflict with such statute shall remain in full force and effect, and all provisions contained herein that do so conflict shall be deemed to be amended so as to provide to JoVE the maximum rights permissible within such statute.

8. Likeness, Privacy, Personality. The Author hereby grants JoVE the right to use the Author's name, voice, likeness, picture, photograph, image, biography and performance in any way, commercial or otherwise, in connection with the Materials and the sale, promotion and distribution thereof. The Author hereby waives any and all rights he or she may have, relating to his or her appearance in the Video or otherwise relating to the Materials, under all applicable privacy, likeness, personality or similar laws.

9. Author Warranties. The Author represents and warrants that the Article is original, that it has not been published, that the copyright interest is owned by the Author (or, if more than one author is listed at the beginning of this Agreement, by such authors collectively) and has not been assigned, licensed, or otherwise transferred to any other party. The Author represents and warrants that the author(s) listed at the top of this Agreement are the only authors of the Materials. If more than one author is listed at the top of this Agreement and if any such author has not entered into a separate Article and Video License Agreement with JoVE relating to the Materials, the Author represents and warrants that the Author has been authorized by each of the other such authors to execute this Agreement on his or her behalf and to bind him or her with respect to the terms of this Agreement as if each of them had been a party hereto as an Author. The Author warrants that the use, reproduction, distribution, public or private performance or display, and/or modification of all or any portion of the Materials does not and will not violate, infringe and/or misappropriate the patent, trademark, intellectual property or other rights of any third party. The Author represents and warrants that it has and will continue to comply with all government, institutional and other regulations, including, without limitation all institutional, laboratory, hospital, ethical, human and animal treatment, privacy, and all other rules, regulations, laws, procedures or guidelines, applicable to the Materials, and that all research involving human and animal subjects has been approved by the Author's relevant institutional review board.

10. JoVE Discretion. If the Author requests the assistance of JoVE in producing the Video in the Author's facility, the Author shall ensure that the presence of JoVE employees, agents or independent contractors is in accordance with the relevant regulations of the Author's institution. If more than one author is listed at the beginning of this Agreement, JoVE may, in its sole discretion, elect not take any action with respect to the Article until such time as it has received complete, executed Article and Video License Agreements from each such author. JoVE reserves the right, in its absolute and sole discretion and without giving any reason therefore, to accept or decline any work submitted to JoVE. JoVE and its employees, agents and independent contractors shall have

jove JOURNAL OF VISUALIZED EXPERIMENTS
1 Alewife Center #200
Cambridge, MA 02140
tel. 617.945.9051
www.jove.com

ARTICLE AND VIDEO LICENSE AGREEMENT

full, unfettered access to the facilities of the Author or of the Author's institution as necessary to make the Video, whether actually published or not. JoVE has sole discretion as to the method of making and publishing the Materials, including, without limitation, to all decisions regarding editing, lighting, filming, timing of publication, if any, length, quality, content and the like.

11. Indemnification. The Author agrees to indemnify JoVE and/or its successors and assigns from and against any and all claims, costs, and expenses, including attorney's fees, arising out of any breach of any warranty or other representations contained herein. The Author further agrees to indemnify and hold harmless JoVE from and against any and all claims, costs, and expenses, including attorney's fees, resulting from the breach by the Author of any representation or warranty contained herein or from allegations or instances of violation of intellectual property rights, damage to the Author's or the Author's institution's facilities, fraud, libel, defamation, research, equipment, experiments, property damage, personal injury, violations of institutional, laboratory, hospital, ethical, human and animal treatment, privacy or other rules, regulations, laws, procedures or guidelines, liabilities and other losses or damages related in any way to the submission of work to JoVE, making of videos by JoVE, or publication in *JoVE* or elsewhere by JoVE. The Author shall be responsible for, and shall hold JoVE harmless from, damages caused by lack of sterilization, lack of cleanliness or by contamination due to the making of a video by JoVE its employees, agents or independent contractors. All sterilization, cleanliness or decontamination procedures shall be solely the responsibility of the Author and shall be undertaken at the Author's expense. All indemnifications provided herein shall include JoVE's attorney's fees and costs related to said losses or damages. Such indemnification and holding harmless shall include such losses or damages incurred by, or in connection with, acts or omissions of JoVE, its employees, agents or independent contractors.

12. Fees. To cover the cost incurred for publication, JoVE must receive payment before production and publication the Materials. Payment is due in 21 days of invoice. Should the Materials not be published due to an editorial or production decision, these funds will be returned to the Author. Withdrawal by the Author of any submitted Materials after final peer review approval will result in a US$1,200 fee to cover pre-production expenses incurred by JoVE. If payment is not received by the completion of filming, production and publication of the Materials will be suspended until payment is received.

13. Transfer, Governing Law. This Agreement may be assigned by JoVE and shall inure to the benefits of any of JoVE's successors and assignees. This Agreement shall be governed and construed by the internal laws of the Commonwealth of Massachusetts without giving effect to any conflict of law provision thereunder. This Agreement may be executed in counterparts, each of which shall be deemed an original, but all of which together shall be deemed to me one and the same agreement. A signed copy of this Agreement delivered by facsimile, e-mail or other means of electronic transmission shall be deemed to have the same legal effect as delivery of an original signed copy of this Agreement.

A signed copy of this document must be sent with all new submissions. Only one Agreement required per submission.

CORRESPONDING AUTHOR:

Name: Rehan Kapadia

Department: Ming Hsieh Department of Electrical Engineering

Institution: University of Southern California

Article Title: Indium Phosphide Synaptic Device on Silicon to Emulate Synaptic Behavior for Neuromorphic Computing

Signature:  Date: 06.21.2018

Please submit a signed and dated copy of this license by one of the following three methods:

1) Upload a scanned copy of the document as a pfd on the JoVE submission site;
2) Fax the document to +1.866.381.2236;
3) Mail the document to JoVE / Attn: JoVE Editorial / 1 Alewife Center #200 / Cambridge, MA 02139

For questions, please email submissions@jove.com or call +1.617.945.9051

USC Viterbi
School of Engineering

Electrical Engineering
Rehan Kapadia
Assistant Professor

8/19/2018

University of Southern California
3737 Watt Way
Los Angeles, CA, 90089

Editor of *Journal of Visualized Experiments*

Dear Editor,

We greatly appreciate your valuable comments to strengthen our manuscript titled "*Indium Phosphide Synaptic Device on Silicon to Emulate Synaptic Behavior for Neuromorphic Computing*". We have revised our manuscript accordingly to address the comments and questions raised. All the changes are tracked in the marked version of the manuscript. Thank you for your time and effort spent on this.

Warmest regards,

Rehan Kapadia
Assistant Professor
Electrical Engineering
University of Southern California
213-821-0845
rkapadia@usc.edu

Click here to access/download;Supplemental File (Figures, Permissions etc.);ACS Nano RightsLink.pdf

Title: Mimicking Biological Synaptic Functionality with an Indium Phosphide Synaptic Device on Silicon for Scalable Neuromorphic Computing

Author: Debarghya Sarkar, Jun Tao, Wei Wang, et al

Publication: ACS Nano

Publisher: American Chemical Society

Date: Feb 1, 2018

Logged in as:
Debarghya Sarkar
Account #:
3001168592

LOGOUT

PERMISSION/LICENSE IS GRANTED FOR YOUR ORDER AT NO CHARGE

This type of permission/license, instead of the standard Terms & Conditions, is sent to you because no fee is being charged for your order. Please note the following:

- Permission is granted for your request in both print and electronic formats, and translations.
- If figures and/or tables were requested, they may be adapted or used in part.
- Please print this page for your records and send a copy of it to your publisher/graduate school.
- Appropriate credit for the requested material should be given as follows: "Reprinted (adapted) with permission from (COMPLETE REFERENCE CITATION). Copyright (YEAR) American Chemical Society." Insert appropriate information in place of the capitalized words.
- One-time permission is granted only for the use specified in your request. No additional uses are granted (such as derivative works or other editions). For any other uses, please submit a new request.

BACK CLOSE WINDOW