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Benjamin Werth
Associate Editor for Chemistry at JoVE
1 Alewife Center, Suite 200
Cambridge, MA 02140

Dear Benjamin,

I am pleased to present an updated version of our article entitled "Sacrificial nanoparticles to remove the effects of shot noise in contact holes fabricated by E-beam lithography," by Moshood K. Morakinyo and I, for publication consideration in JoVE.

In this work, we exploit recent rapid advances in the synthesis and isolation of monodisperse nanostructures, as templates to develop sub 20nm electrical contacts for transistor source and drain. As the size of the transistor gate continues to shrink the corresponding source and drain contacts must shrink proportionately. At the current level of technology, approaching 14nm gate lengths, new effects emerge and degrade the overall yield of fabrication. Chief amongst them are the line-edge roughness (LER) and size fluctuation arising from the statistical fluctuations in number of photons/reactive molecules in a given nanoregion (the so-called shot noise(SN) effect).

The science behind the method is based on the electrostatic funneling to direct charged nanostructures to the center of the patterns in photoresist polymer thin films. Once anchored, the nanostructures provide a template that could reshape pattern in the resist film using surface tension effect. Specifically the method integrates top-down and bottom-up processing steps involving: (a) rough lithographic patterning, (b) size/shape selected nanostructure deposition, (c) resist reflow around the nanostructures, and (d) selective removal/etching of the nanostructures.

The significance of the work includes the following.

(1) It is compatible with the standard VLSI processing and hence potentially adaptable in high volume manufacturing.

(2) Any reflowable resist can be used for this type of patterning.

(3) Effects of shot noise (observed in optical, e-beam, X-ray, EUV lithography) and line edge roughness (SN/LER) are removed using size-controlled nanostructures.

(4) One specific application of the method discussed in the letter describes patterning vias for transistor source and drain contacts using nanoparticles.

(5) Wide range of nanomaterials based on metals, insulators and semiconductors can be used as long as they can be selectively etched.

As this work is interdisciplinary, I have suggested reviewers well versed in both technological and scientific aspects of this type of applied research including, a physicist, an electrical engineer and a chemist.

The work was conducted at the Portland State University supported by Intel Corporation. The e-beam fabrication was performed at the CAMCOR user facility located at the University of Oregon which was supported by ONAMI (Oregon Nanoscience And Microtechnolgy Institute) . Portland State University has filed a patent based on this work; however, neither I or my student has any financial conflict of interest with respect to this work. Please let me know if you need any additional information. Best regards,

7/1/2016

X 

Shankar B. Rananavare
Research Associate Professor
Signed by: Shankar Balalasaheb Rananavare