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Writing and Low-Temperature Characterization of Oxide Nanostructures

--Manuscript Draft--

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Abstract:	Oxide nanoelectronics is a rapidly growing field which seeks to develop novel materials with multifunctional behavior at nanoscale dimensions. Oxide interfaces exhibit a wide range of properties that can be controlled include conduction, piezoelectric behavior, ferromagnetism, superconductivity and nonlinear optical properties. Recently, methods for controlling these properties at extreme nanoscale dimensions have been discovered and developed. Here are described explicit step-by-step procedures for creating LaAlO3/SrTiO3 nanostructures using a reversible conductive atomic force microscopy technique. The processing steps for creating electrical contacts to the LaAlO3/SrTiO3 interface are first described. Conductive nanostructures are created by applying voltages to a conductive atomic force microscope tip and locally switching the LaAlO3/SrTiO3 interface to a conductive state. A versatile nanolithography toolkit has been developed expressly for the purpose of controlling the atomic force microscope (AFM) tip path and voltage. Then, these nanostructures are placed in a cryostat and transport measurements are performed. The procedures described here should be useful to others wishing to conduct research in oxide nanoelectronics.
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Cover Letter

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Dear Editor,

Enclosed please find our video manuscript, entitled "Writing and Low-Temperature Characterization of Oxide Nanostructures", which we are submitting for publication in JoVE. The manuscript and video describe a process that is central to more than a dozen published works in Science, Nature Materials and other high-profile journals. Despite all of the documented results, there still does not exist an archival-quality visual description of how we prepare our nanostructures. That is the explicit aim of this video manuscript.

I am highly supportive of the JoVE mission, and routinely use video in my laboratory for a variety of purposes. We chose to use an author-submission because we believe that we have the in-house capability to produce a video that meets the standards of JoVE. If there are technical problems with the video, it is not due to a lack of ability on our side, but rather lack of appreciation of some subtleties that should easily be correctable (we hope).

I do have a question that was not answered on the website: can we upload a manuscript on arxiv.org? This practice is common for other journal submissions, and ends up improving the final published manuscript. We believe that an arxiv post will serve the same purpose for JoVE. If this practice is not allowed, I would appreciate knowing.

Sincerely,

Jeremy Levy

Title: Writing and Low-Temperature Characterization of Oxide Nanostructures.

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Short Abstract:
Oxide nanostructures provide new opportunities for science and technology. The interfacial conductivity between $LaAlO_3$ and $SrTiO_3$ can be controlled with near-atomic precision using a conductive atomic force microscopy technique. The protocol for creating and measuring conductive nanostructures at $LaAlO_3/SrTiO_3$ interfaces is demonstrated.

Long Abstract:
Oxide nanoelectronics is a rapidly growing field which seeks to develop novel materials with multifunctional behavior at nanoscale dimensions. Oxide interfaces exhibit a wide range of properties that can be controlled include conduction, piezoelectric behavior, ferromagnetism, superconductivity and nonlinear optical properties. Recently, methods for controlling these properties at extreme nanoscale dimensions have been discovered and developed. Here are described explicit step-by-step procedures for creating $LaAlO_3/SrTiO_3$ nanostructures using a reversible conductive atomic force microscopy technique. The processing steps for creating electrical contacts to the $LaAlO_3/SrTiO_3$ interface are first described. Conductive nanostructures are created by applying voltages to a conductive atomic force microscope tip and locally switching the $LaAlO_3/SrTiO_3$ interface to a conductive state. A versatile nanolithography toolkit has been developed expressly for the purpose of controlling the atomic force microscope (AFM) tip path and voltage. Then, these nanostructures are placed in a cryostat and transport measurements are performed. The procedures described here should be useful to others wishing to conduct research in oxide nanoelectronics.

Introduction:

Oxide heterostructures[1-5] exhibit a remarkably wide variety of emergent physical phenomena which are both scientifically interesting and potentially useful for applications[4]. In particular, the interface between $LaAlO_3$ (LAO) and $SrTiO_3$ (STO)[6] can exhibit insulating, conducting, superconducting[7], ferroelectric-like[8], and ferromagnetic[9] behavior. In 2006, Thiel et al showed[10] that there is a sharp insulator-to-metal transition as the thickness of the LAO layer is increased, with a critical thickness of 4 unit cells (4uc). It was subsequently shown that 3uc-LAO/STO structures exhibit a hysteretic transition that can be controlled locally with a conductive atomic-force microscope (c-AFM) probe[11].

The properties of oxide interfaces such as $LaAlO_3/SrTiO_3$ depend on the absence or presence of conducting electrons at the interface. These electrons can be controlled using top gate electrodes [12,13], back gates [10], surface adsorbates[14], ferroelectric layers[15,16] and c-AFM lithography[11]. A unique feature of c-AFM lithography is that very small nanoscale features can be created.

Electrical top gating, combined with two-dimensional confinement, is often used to create quantum dots in III-V semiconductors [17]. Alternatively, quasi-one-dimensional semiconducting nanowires can be electrically gated by proximity. The methods for producing these structures are time-consuming and generally irreversible. By contrast, the c-AFM lithography technique is reversible in the sense that a nanostructure can be created for one experiment, and then "erased" (similar to a whiteboard). Generally, c-AFM writing is performed with positive voltages applied to the AFM tip, while, erasing is performed using negative voltages. The time required to create a particular structure depends on the complexity of the device but is usually less than 30 minutes; most of that time is spent erasing the canvas. The typical spatial resolution is about 10 nanometers, but with proper tuning features as small as 2 nanometers can be created[18].

A detailed description of the nanoscale fabrication procedure follows. The detail provided here should be sufficient to allow similar experiments to be performed by interested researchers. The method described here has many advantages over traditional lithographic approaches used to create electronic nanostructures in semiconductors.

The c-AFM lithography method described here is part of a much broader class of scanning-probe-based lithography efforts, including scanning anodic oxidation[19], dip-pen nanolithography[20], piezoelectric patterning[21], and so on. The c-AFM technique described here, coupled with the use of novel oxide interfaces, can produce some of the highest-precision electronic structures with an unprecedented variety of physical properties.

Protocol:

1. Obtain LAO/STO heterostructures

1.1) Obtain an oxide heterostructure consisting of 3.4 unit cells of LAO grown by pulsed laser

deposition on TiO_2-terminated STO substrates. Details of sample growth are described in Ref. [22].

2. Photolithographic processing of samples

Create electrical contacts to the LAO/STO interface, with bonding pads for wiring canvases to a chip carrier. The individual processing steps **Error! Reference source not found.**are described in detail below.

2.1) Spin photoresist

2.1.1) Spin photoresist on the samples at 600 rpm for 5 s, then at 4000 rpm for 30 s. The photoresist layer will be about 2 µm thick. Bake the samples at 95° for 1 minute.

2.2) Expose photoresist using a mask aligner with 320 nm light for 100 s with a dose of 5 mW/cm^2.

2.3) Develop the photoresist in photoresist developer for one minute.

2.4) Ion milling

2.4.1) Use an Ar^+ ion mill to remove 15 nm of material (LAO and STO) in the areas not covered by photoresist. Place the samples at a 22.5° angle to the direction perpendicular to the incoming Ar+ ion beam. If the Ar+ etching rate is not calibrated, perform a calibration run to ensure that the correct amount of material is removed. Determine the etching depth using AFM or equivalent profilmetry.

2.5) DC sputtering of Ti and Au

2.5.1) Deposit 4 nm Ti, then 25 nm Au onto the samples so that the Au makes electrical contact with the exposed STO layer. The sputtering pressure is in the range 2-6 x 10^{-7} Torr, and the sputtering takes place with the sample at room temperature. Pre-sputter Ti for 10 minutes with shutter closed at 100 W, then open shutter and sputter for 20 s at 100 W. Upon completion, immediately pre-sputter Au for 1 minute at 50 W then sputter Au for 30 seconds to the samples at 50 W. Calibrate the time to produce the desired Ti and Au thicknesses.

2.6) Lift-off

2.6.1) Use Acetone/IPA ultrasonic wash to remove photoresist from the surface of the samples.

2.7) Second layer

2.7.1) A second lithographic process, excluding step 4 (i.e., excluding ion milling), is used to create gold wire connections to individual bonding pads. The two patterns must be well-

aligned to ensure that they do not produce electrical shorts.

2.8) Plasma cleaning.

2.8.1) An IPC Barrel Etcher is used to remove the photoresist residue in the pattern trench. The instrument used at the 100 W and 1 Torr argon for 1 minute.

3. Wire bond a sample to prepare for writing

3.1) Mount the LAO/STO sample in a chip carrier (Figure 2a**Error! Reference source not found.**) with 28 available pins.

3.2) Wire bond structure

NOTE: Use a wire bonder to make electrical connections between bonding pads on the sample and the chip carrier. Attach 1 mil (25 micrometer) gold wires between the electrical contacts and the chip carrier.Write nanostructures

4. Write nanostructures.

4.1) Create an informal sketch of the conductive nanostructure (Figure 3**Error! Reference source not found.**A).

4.2) Open the scalable vector graphics (SVG) editor (Figure 3**Error! Reference source not found.**B).

4.2.1) Use a template or define the window size to match that of the AFM image.

4.2.2) Load the AFM image of the sample into the SVG editor.

4.2.3) Create nanostructure elements overlaid on the AFM image.

4.3) Load the SVG file into the nanolithography program.

4.4) Run the lithography software to create a conductive nanostructure.

4.4.1) Use V_{tip}=+10 V to create nanostructures, and V_{tip}=-10 V to erase nanostructures.

4.4.2) Move the c-AFM tip at a speed ranging from 200 nm/s to 2 μm/s.

5. Cool device and take measurements

5.1) Turn off all white lights and use red filters/light sources.

5.2) Extract the sample from the AFM system.

5.3) Load the sample into the dilution refrigerator (Figure 5A).

5.4) Measure resistance vs. temperature (Figure 5B) as the sample is cooled.

5.5) Measure transport properties at low temperatures (Figure 5C).

Representative Results:

The results shown here are representative of the transport behavior that can be exhibited by this class of nanostructures, and has been described elsewhere in detail[23-26]. In this example, a nanowire cavity has been constructed (Figure 4) from a 3.3 unit cell LAO/STO heterostructure. Conductive paths (shown in green) are typically 10 nm wide, as determined by nanowire "cutting" experiments[11]. The tip speed and voltage for each segment is independently configurable from the lithography front panel (Figure 4B), as is the tip writing speed. "Virtual electrodes" that interface with the interfacial contacts ensure that there is a highly conductive electrical connection to the nanostructures.

After the nanostructure is written, it is transferred to the dilution refrigerator. Exposure to light at or below 550 nm will produce unwanted photoconduction, so it is important to transfer the device in darkness or with the aid of a red "darkroom" light (Figure 5A). Electrical connections should be made at room temperature, and as with most semiconductor nanostructures, great care should be taken when changing electrical connections at cryogenic temperatures. If the devices is subjected to electrostatic discharge, it will most likely become insulating. Remarkably, the device functionality can be recovered by "cycling" the temperature to 300K and cooling down again.

During cooldown, it is routine to monitor the two-terminal resistance, and even the four-terminal resistance, as a function of temperature. For these measurements an ac voltage (typically ~$1\ \mathrm{mV}$) is applied at a low frequency (<10 Hz) to one of the electrodes, while the ac current is measured using a transimpedance amplifier. Lock-in demodulation and filtering is performed using a home-developed lock-in amplifier. The ac current is monitored as a function of temperature (Figure 5B).

Once the device is cooled to the base temperature of the dilution refrigerator (50 mK), four-terminal transport measurements are performed (Figure 5C). For these measurements, current is sourced through the main channel of the device, while voltage across the device is simultaneously measured. Instead of measuring with a lock-in amplifier, a full current-voltage (I-V) trace is measured. This method contains more information and the differential conduction can be calculated via numerical differentiation. For the particular device, the differential conduction is measured as a function of the side-gate voltage V_{sg}. This gate allows the chemical

potential of the device to be changed. The transport through the device shows a strong non-monotonic dependence, indicating regions in which Coulomb blockade takes place for smaller values, and strong superconductivity for larger values of V_{sg} . Details about the physical interpretation for this class of device will be described elsewhere.

Figure Legends:

Figure 1. Photolithographic processing steps. Step 1: spin photoresist. Step 2: expose photoresist using mask aligner. Step 3: develop photoresist. Step 4: ion milling. Step 5: DC sputtering to deposit Ti and Au. Step 6: lift-off. Step 7: deposit the second layer. Step 8: plasma cleaning.

Figure 2. Images of lithographically patterned LAO/STO heterostructures. A. Image showing 5mm x 5mm sample wire bonded to a chip carrier. B. Optical image showing bonding pads and one of the canvases. C. Close-up of a single canvas.

Figure 3. A. Informal design of LAO/STO nanostructure. B. Precise layout of nanostructure using an open-source scalable vector graphics (SVG) editor.

Figure 4. Lithography front panel for c-AFM patterning. B. Screenshot from 3D simulator showing position and voltage of c-AFM tip.

Figure 5. A. LAO/STO nanostructure being inserted into dilution refrigerator. B. Monitoring of sample resistance as it is cooled from 300K to 50 mK. C. Monitoring of four-terminal differential conductance of device as a function of side gate voltage Vsg and voltage across the device (V4t). Intensity graph displayed in units of siemens (S), and voltages are displayed in units of volts (V).

Discussion:

Successful creation of nanostructures depends on several critical steps. It is important that the LAO/STO samples are grown with a thickness that is known to be at the boundary between the insulating and conductive phase. (Details of sample growth fall outside the scope of this paper, but are crucial for overall success.) Second, it is important to have relative humidity within the range 25-45% for successful c-AFM writing. Values below 25% are unlikely to produce conductive nanostructures, while too high humidity will generally produce uncontrollably large features. Also, temperature control of the AFM is important if the c-AFM tip needs to achieve precise registry over long periods of time. Once the nanostructures are created, they must be placed in a vacuum environment if experiments lasting longer than a few hours are to be performed. For the experiments described here, the structure is created and within minutes transferred to a vacuum environment.

It is recommend before writing that a “writing test” be performed on all relevant electrodes. In such a test, two virtual electrodes are first created, and a single nanowire is written while

simultaneously monitoring the conductance. A similar test of erasure can be performed by "cutting" the nanowire shortly afterwards. If the nanostructure is decaying rapidly, the issue is most likely due either to the interfacial contacts or the canvas itself. To distinguish between these two effects, a four-terminal measurement of the conductance should be performed, and the two-terminal conductance should be compared with the four-terminal conductance as a function of time. If the two-terminal conductance is decaying more rapidly than the four-terminal conductance, then the issue is related to the electrical contacts to the interface. If the four-terminal conductance is decaying at a comparable rate, then most likely the canvas is not suitable and should be replaced.

There are natural limitations of the current method for creating nanostructures. Specifically, the writing speed for the smallest devices is limited to a few hundred nanometers per second. Speeds far above that value lead to unpredictable results. Use of parallel writing techniques are possible[27,28], but are not highly developed and have their own drawbacks. The size of nanostructures that can be created is naturally limited by the scan range of the AFM being used. A high-quality AFM with closed-loop feedback in the two scan directions is highly recommended. Tracking of point-like objects on the sample surface should be performed to monitor temporal drift of the sample.

Once creation of conductive nanostructures at oxide interfaces has been mastered, there are a wide range of experimental directions that can be explored. Using this technique, a wide variety of nanostructures and devices have already been demonstrated, including nanowires[18], tunnel barriers[29], rectifying junctions[30], field-effect transistors[18], single-electron transistors[31], superconducting nanowires[32], nanoscale optical detectors[33], and nanoscale THz emitters and detectors[34].

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Disclosures:
The authors have nothing to disclose.

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Figure 1
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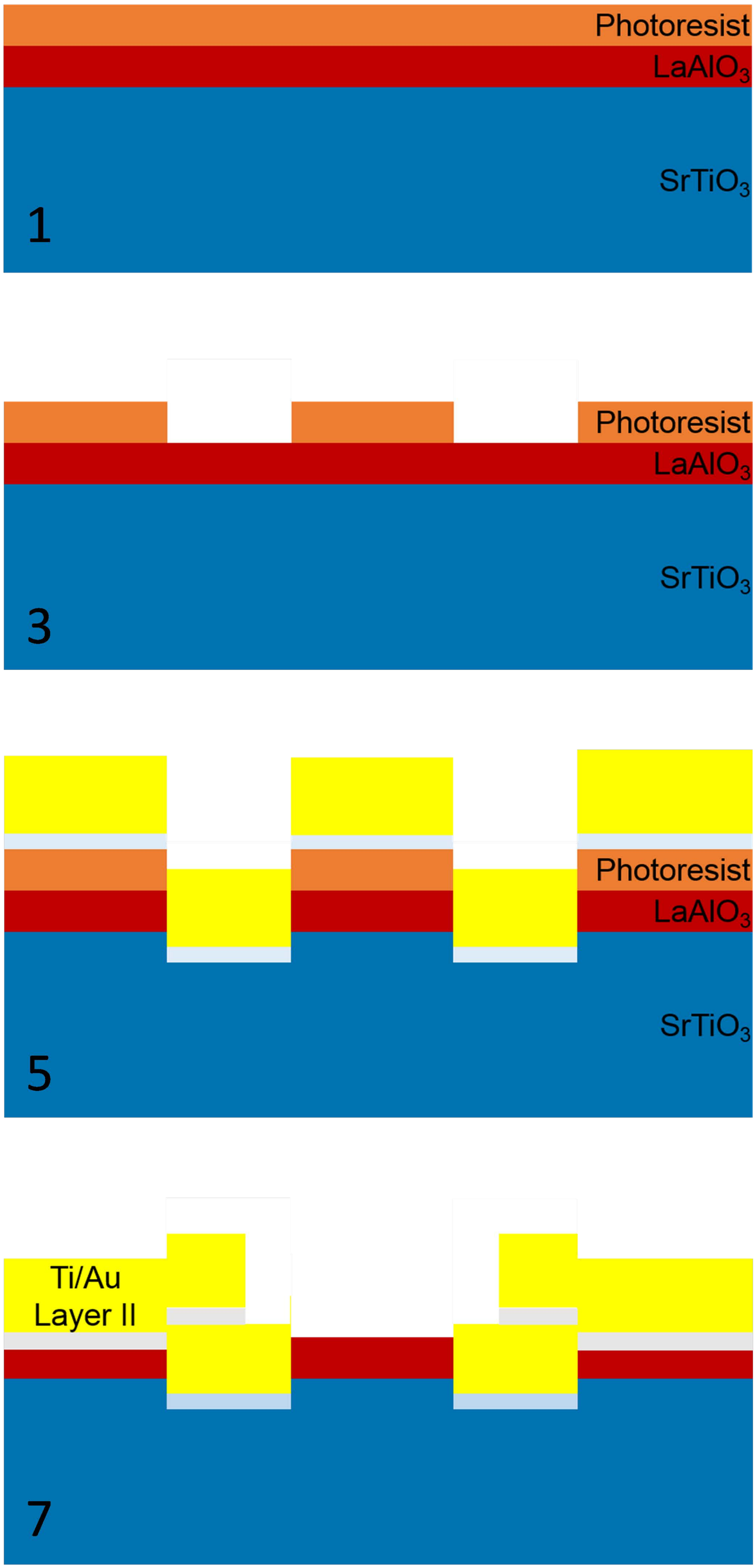

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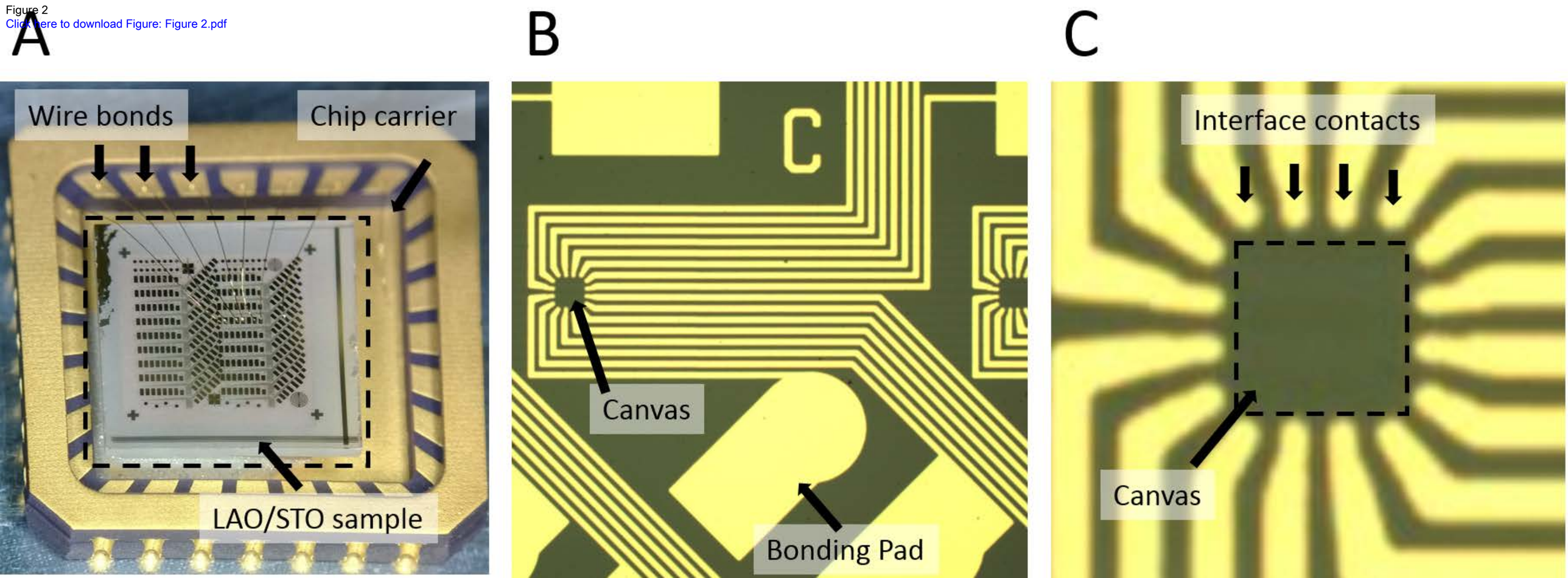

Figure 3

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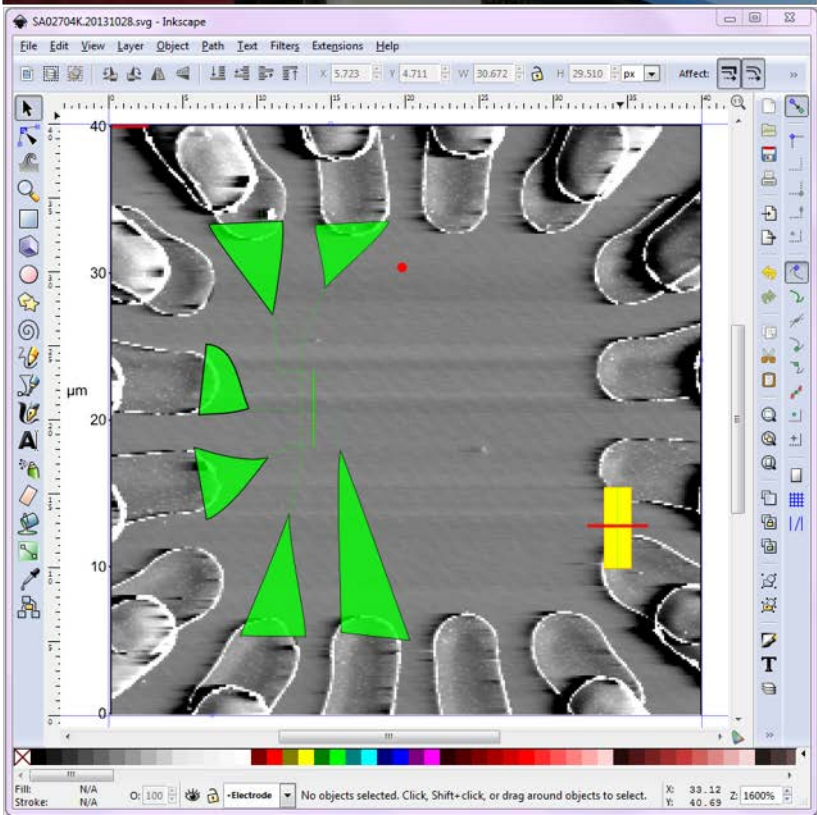

Figure 4
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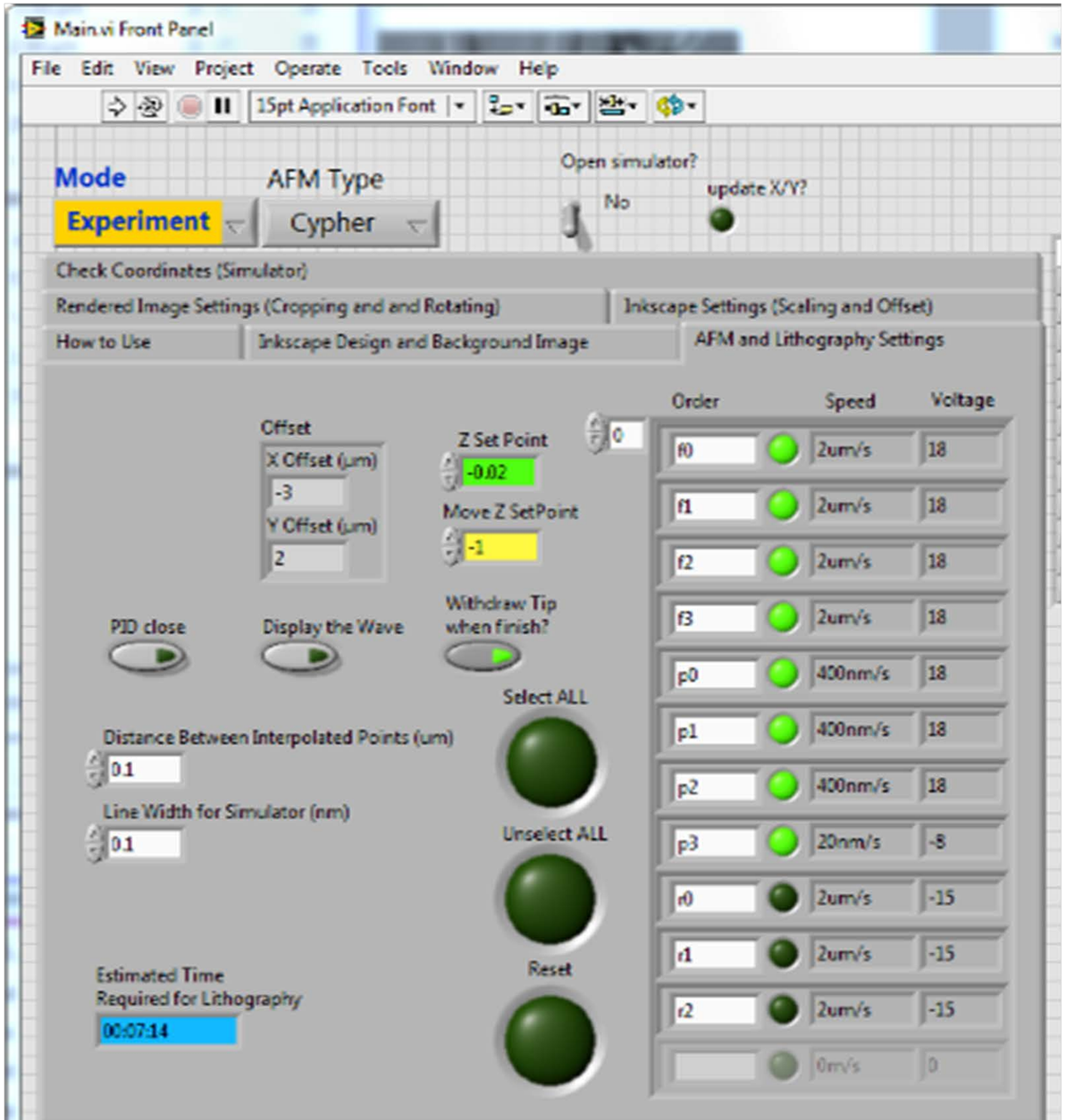

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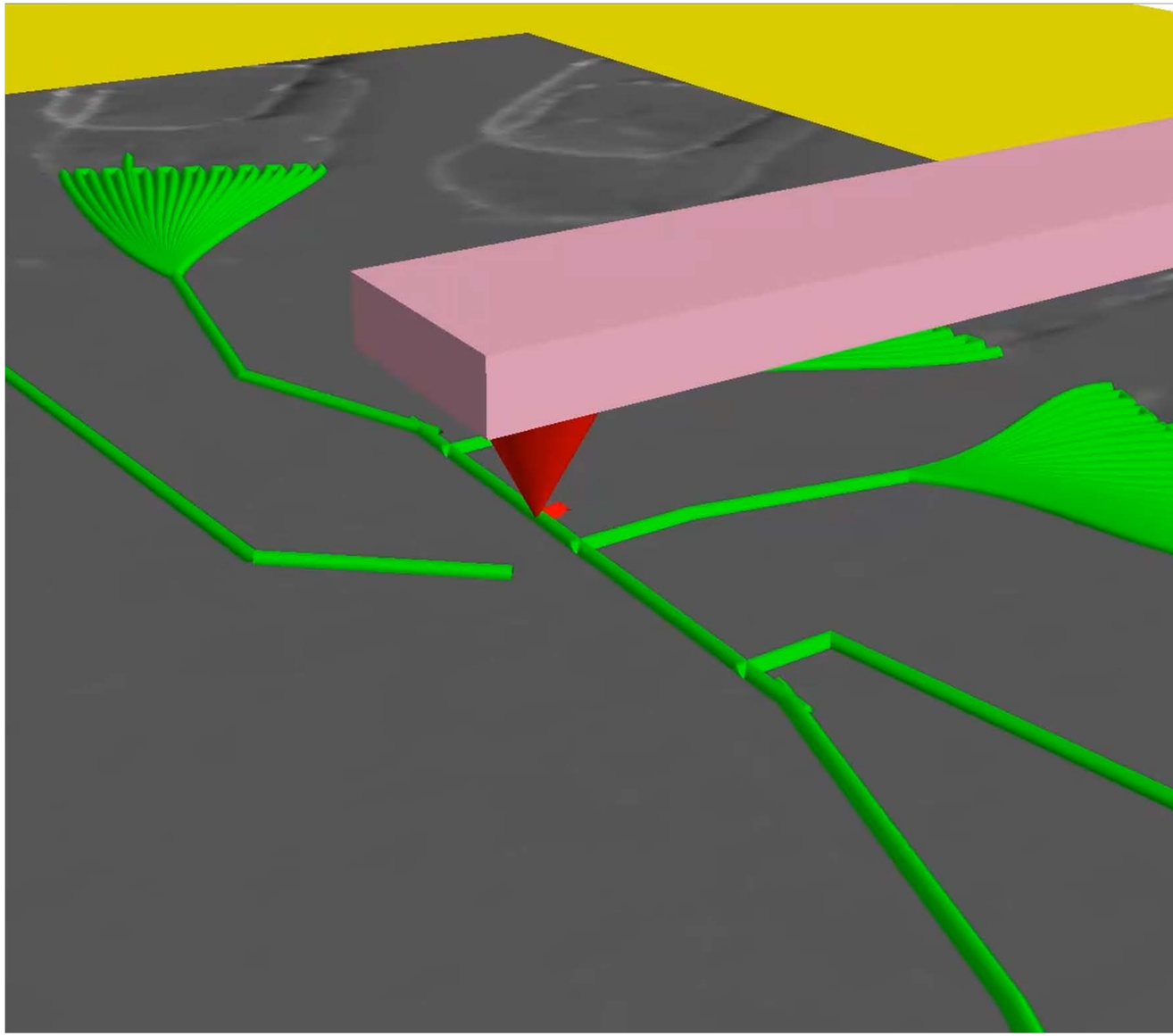

Figure 5

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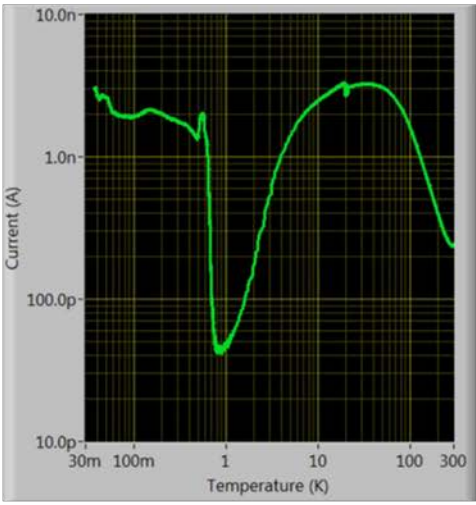
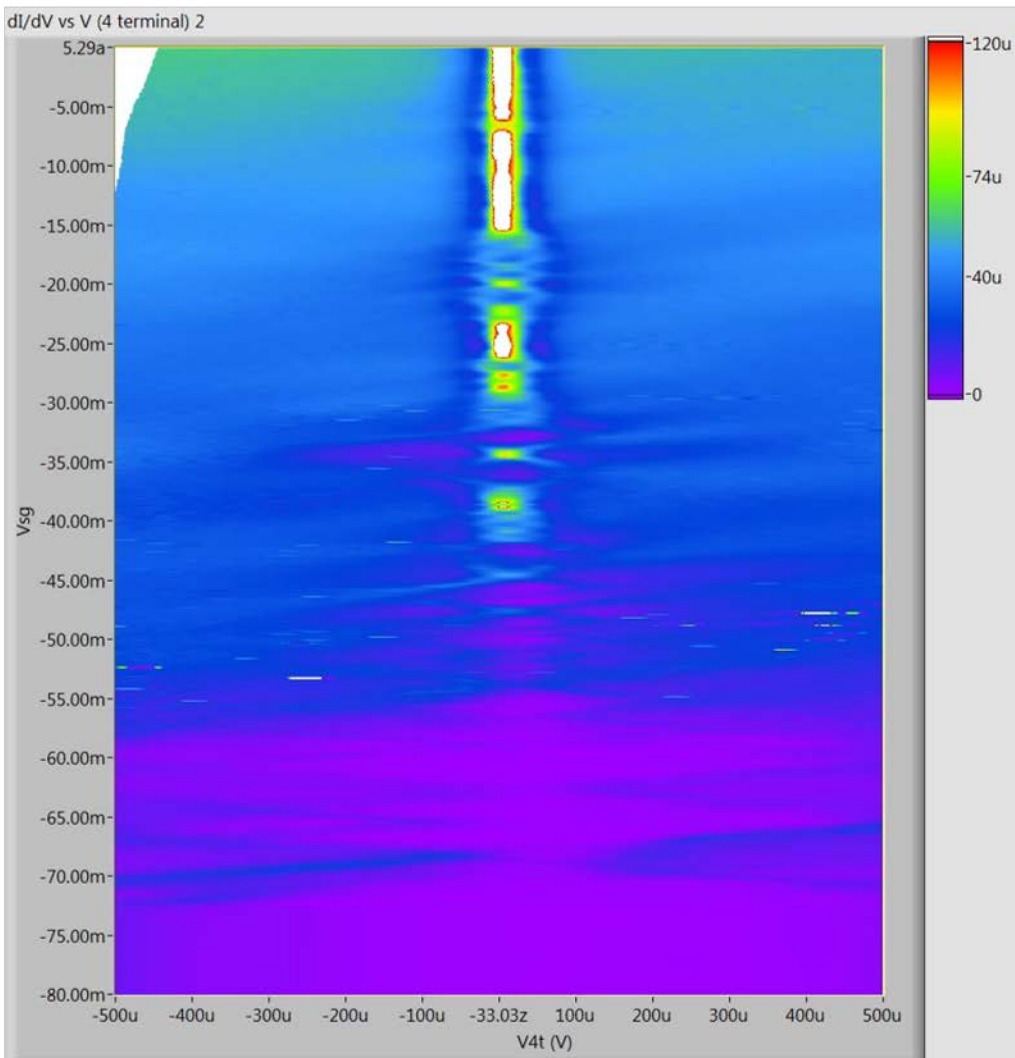
A

B



C



Excel Spreadsheet- Table of Materials/Equipment

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Name	Company	Catalog Number
Equipment		
Contact Aligner	Karl-Suss	MA6
Spinner	Solitec	5110C
Ion Mill	Commonwealth Scientific	8C
Sputtering System	Leybold-Heraeus	Z-650
Barrel Etcher	Branson/IPC	3000C
Wire Bonder	Westbond	7700E
AFM	Asylum Research	MFP-3D
Dilution Refrigerator	Quantum Design	P850
Ultrasonic Wash Machine	Fisher Scientific	15-335-6
Current Amplifier	Femto	DLPCA-200
Materials		
LaAlO3/SrTiO3	Prof. Chang-Beom Eom	N/A
Photoresist	AZ Electronic Materials	P4210
Developer	AZ Electronic Materials	400K
Acetone	Fisher Scientific	A929SK-4
Isopropyl Alcohol	Fisher Scientific	A459-1
Deionized Water	Fisher Scientific	23-290-065
Gold Wire	DuPont	5771
Chip Carrier	NTK Technologies	IRK28F1-5451D

Comments

5mm x 1mm with ~3.4 unit cells of LAO (See Reference 18)

1 mil diameter

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Title of Article: Writing and Low-Temperature Characterization of Oxide Nanostructures

Author(s): Akash Levy, Feng Bi, Mengchen Huang, Shicheng Lu, Michelle Tomczyk, Guanglei Cheng, Patrick Irvin, Jeremy Levy

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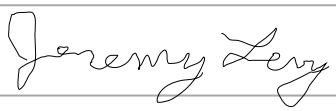
Signature:	 Date: 19 Dec 2013

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We thank the Reviewers and Editor for their constructive comments. Below please find our responses to each comment.

Editorial comments:

1)Audio issues:
•2:53-3:31 – The audio here is lower than the rest of the voice-over in the video. It should be normalized.

We have fixed the audio issues.

2)Please make sure that your references comply with JoVE instructions for authors. In-text formatting: corresponding reference numbers should appear as superscripts after the appropriate statement(s) in the text of the manuscript. Citation formatting should appear as follows: (For 6 authors or less list all authors. For more than 6 authors, list only the first author then *et al.*): [Lastname, F.I., LastName, F.I., LastName, F.I. Article Title. *Source*. **Volume** (Issue), FirstPage – LastPage, doi:DOI, (YEAR).]

We have corrected the format of the references. Regarding Reference 1, that article is in press and we expect it to have full coordinates shortly (probably on the time scale for publication of this article if it is accepted).

3)Please take this opportunity to thoroughly proofread your manuscript to ensure that there are no spelling or grammar issues. Your JoVE editor will not copy-edit your manuscript and any errors in your submitted revision may be present in the published version.

Thank you we have made some minor corrections to spelling and grammar.

Reviewers' comments:

Reviewer #1:
Manuscript Summary:
In this article, the authors demonstrate an approach to create and characterize low dimensional oxide structures. This is of great importance to the emerging field of oxide nano-electronics/spintronics. Actually, it should also be potentially applicable to other non-oxide material systems, as long as there is resistance hysteresis behavior. Additionally, I also enjoyed watching the video manuscript.

Major Concerns:
There is no major concern in this version.

Minor Concerns:

However, there are a number of things required to be corrected or improved. I list them below:
1. Keywords. In order to match the title, "oxide nanostructures" is a better keyword than "oxide semiconductor";
We have made this change.

2. Short abstract. In the first sentence, replace "oxide interfaces" by "oxide nanostructures", because "interface" will be difficult to pick up immediately for general audience without introducing it.
We have made this change.

3. Long abstract. In line 77, the "AFM" abbreviation is not defined yet.
We replaced the abbreviation with “atomic force microscope”

4. Line 123 in Protocol & line 195 in Representative Results. There is inconsistency about LaAlO3 (LAO) thickness. In these two lines, LAO are 3.3 unit cells. However, in video and the final comment, LAO are 3.4 unit cells. This typo should be corrected.
We have corrected step 2, which now states “3.4 unit cells”.

5. There are at least four places with texts of "Error! Reference source not found.". I believe they are figure references. If they are not about Figures, figure references should be properly included there.
The unlinked referenes have been corrected.

6. There are occasionally typos. In line 213, space should be added before "mV". In line 172, it should be"Use", not "Us".
Both typos have been corrected.

7. In line 228, add representative references about "other publications"
The sentence now reads: “Details about the physical interpretation for this class of device will be described elsewhere.”

8. The reference format is very odd to me. There are seems like a lot of format errors. Just an example, some are with DOI, some not.

Thank you for pointing out these inconsistencies. They have been corrected in the revised manuscript.

9. In figure 2, it is much better to add more labels to describe A and C.

We have added more labels.

10. Figure 5's Axis labels need to be improved. The Vsg axis is lack of unit of V. For the V4t axis, "-33.03z" is better replaced by "0" or "0u". Move "dI/dV" label closer to color bar and assign a unit to it.

The images shown here are screen captures of the actual display used in the experiment (they appear this wa in the video). We have added information about the units for all of the quantities and corrected the description of the quanitity (differential conductance rather than differential resistance).

Additional Comments to Authors:
There is no additional comments to Authors.

Reviewer #2:
The movie and manuscript JoVE51886R3 by Akash Levy et. al. describe the process of creating conductive nanostructures by applying voltages to a conductive atomic force microscope tip and locally switching the LaAlO3/SrTiO3 interface to a conductive state. The goal of this publication is to provide a detailed description of how these conductive nanostructures are created and measured. The details provided here should are sufficient to allow similar experiments to be performed using this technique.

I think that this work is well presented and deserves to be published in the Journal of Visualized Experiments (JoVE). However, there are some issues that should be addressed prior to publishing this work.

General Comments:

1) Some editing is required in order to make stronger and more concise statements.

We have attempted to make the language of the manuscript stronger and more concise.

2) References for the figures are not found.

The figures are not taken from other publications.

3) There is no detailed description of how the structure can be erased, although it is mentioned as one of the key features of this technique in the introduction, and very briefly shown in the movie.

Thank you for pointing out this missing information. We have added a description of the erasing procedure: “Generally, c-AFM writing is performed with positive voltages applied to the AFM tip, while, erasing is performed using negative voltages. “

4) Since the sputtering was described in details, the manuscript should include details, or at least a reference to the parameters used in the c-AFM such as applied voltage, scan speed etc.

We have included some typical parameters in the nanostructure writing receipe.

5) There is no conclusion section in the paper and the conclusion section in the video is insufficient. The last paragraph (line 281) states that "wide range of experimental directions that can be explored". Please elaborate.

It is our understanding that the last section should be for "Discussion" rather than conclusion. We have removed the last sentence to focus on the wide family of devices that have already been demonstrated.

6) This description could be upgraded by including some level of discussion of the physics involved, to set this work in its context. The extent of this discussion depends on the editor and the preference for this journal. For example – there is no mention of the basic physics that makes this writing possible. Why do voltages have such an effect on the LAO/STO surface?

We felt that the main purpose of this video article was to describe the methods used to create the structures. Deeper discussion of the basic physics of the devices, or even the writing process itself, has been the subject of other publications (e.g., Ref. 21).

7) The level of details in the various sections is not proportional (e.g. in section 4 – no details about the writing parameters vs. too many details about opening files)

We have included more details about the writing parameters.

Specific Comments:
Editing is needed in the following examples:
76-80: Please revise this section to make a stronger statement or a stronger argument for this publication.

The purpose of the publication is to describe methods by which LAO/STO structures are created and measured. The lines 76-80 are summarizing a process that is described in more detail in the manuscript and illustrated visually in the video. The last sentence (79-80) makes it clear to the reader the scope of the manuscript and the video, and (we hope) will facilitate the process of replicating these results in other laboratories.

108: "…are created is presented" rephrase.

We have rephrased the sentence to read: “A detailed description of the nanoscale fabrication procedure follows.“

152: " Calibrate the times should to produce the desired Ti and Au thicknesses." – remove “should”.

We have fixed this sentence which now reads: “The times should be calibrated to produce the desired Ti and Au thicknesses.”

Line 187: consider switching with line 186

Yes, those parts were written out of order--we have swapped them.

Additional references needed for the following statements:
99: "…is often used to create quantum dots in III-V semiconductors."

We added a representative reference.

Error in figure references: Lines: 130, 169, 177, 178.

We have corrected these errors.

Figure 2: scale bar is missing in the microscope pictures

Additional information to consider including:
143: what is in the calibration run? (AFM? Elipsometry? Profilometry?).

We have added information: “If the Ar+ etching rate is not calibrated, a calibration run should be performed to ensure that the correct amount of material is removed. Etching depth should be determined using AFM or equivalent profilmetry.”

Is the process repeatable and stable?
147: what is the sputtering pressure? Temperature? (Room temperature should also be stated for clarity).

We include this information now:

Deposit 4 nm Ti, then 25 nm Au onto the samples so that the Au makes electrical contact with the exposed STO layer. The sputtering pressure is in the range 2-6 x 10^{-7} Torr, and the sputtering takes place with the sample at room temperature. Pre-sputter Ti for 10 minutes with shutter closed at 100

W, then open shutter and sputter for 20 s at 100 W. Upon completion, immediately pre-sputter Au for 1 minute at 50 W then sputter Au for 30 seconds to the samples at 50 W. The times should be calibrated to produce the desired Ti and Au thicknesses.

Video Comments:

• There is a bit of a problem with the sound between minute 03:00 to 03:35 the voice in the video is much quieter and less understood

We corrected the sound issues, thank you for pointing them out.

• The conclusion should be expanded. Suggestions: speak about the versatility of this technique and about future applications.

Our principal aim for this publication was to describe the methods rather than provide enormous detail about all of the possible structures that could be created. The manuscript itself references a large number of devices that have already been created.